Plasma-dicing: a device-enabling technology for advanced packaging and 3D integration.

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MINAPAD
Session: Dicing / Picking 1
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Kiru · Kezuru · Migaku Technologies

Outline

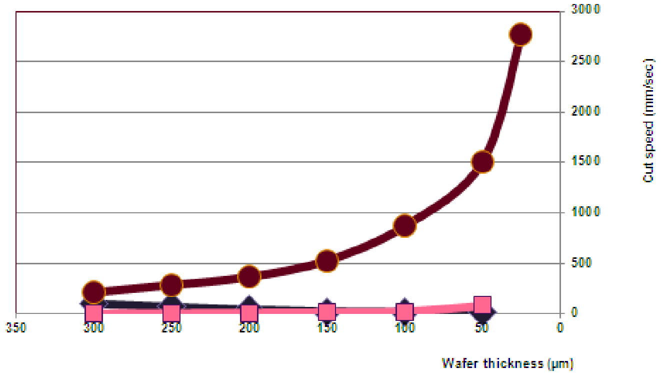
1. Limitations of the current dicing technologies and motivations

2. Integrating Plasma dicing in a 3D packaging flow.

1. Limitations of the current dicing technologies and motivations

2. Integrating Plasma dicing in a 3D packaging flow.

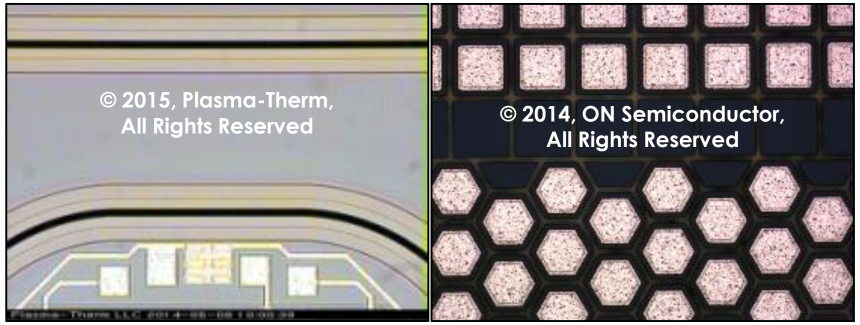
Motivations – What do we want?



1. Throughput

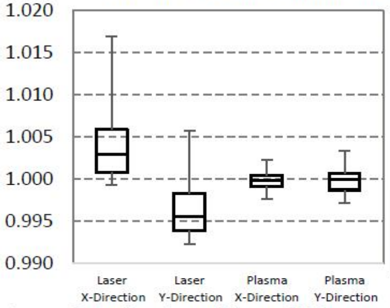
Oxide, nitride,
PR, polyimide,
PBO, metals

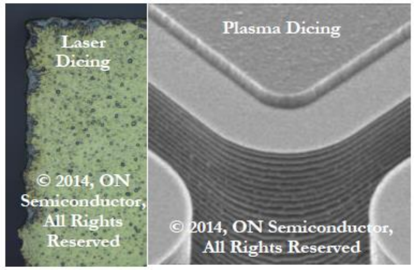
2. Materials



3. Shapes

1x1mm Die Size Variation Comparison
Between Laser and Plasma Dicing





Source: OnSemiconductor, Arizona, 2014

4. Perfect Die

Identifying bottlenecks for throughput

$$Good\ dies\ per\ wafer\ per\ hour$$
$$=$$
$$Y\ .\ N\ .\ W$$

Yield is affected
by dicing
(damages, residues)

Number of dies per wafer

- ✓ Die dimension
- ✓ Die shape
- ✓ Die layout (orthogonal or not)
- ✓ Width of dicing streets

Determined by dicing technology.

Wafers per hour

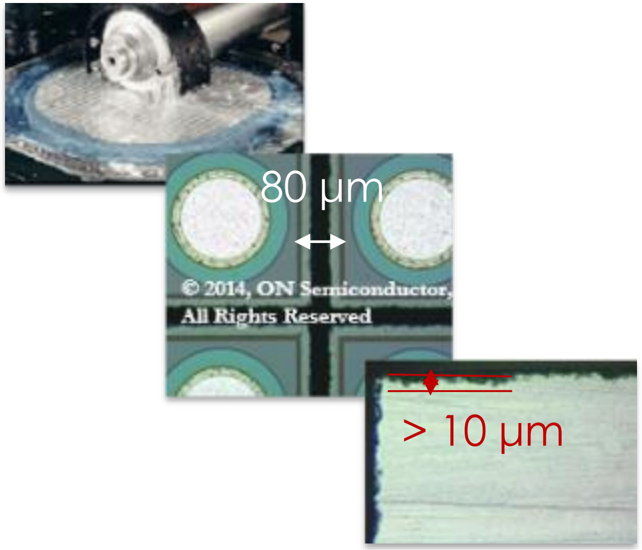
- ✓ Number of process steps
- ✓ Process step time

Cut speed has to be high with
minimal addition of required steps.

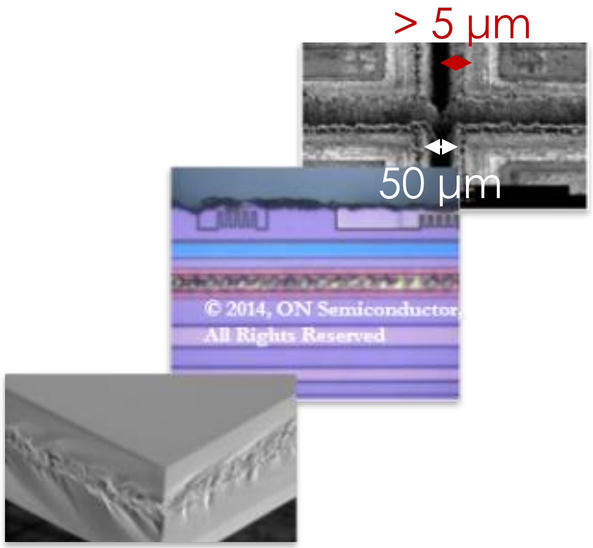
Dicing is a primary bottleneck for throughput

Plasma-Therm

Wafer Dicing Technology limits



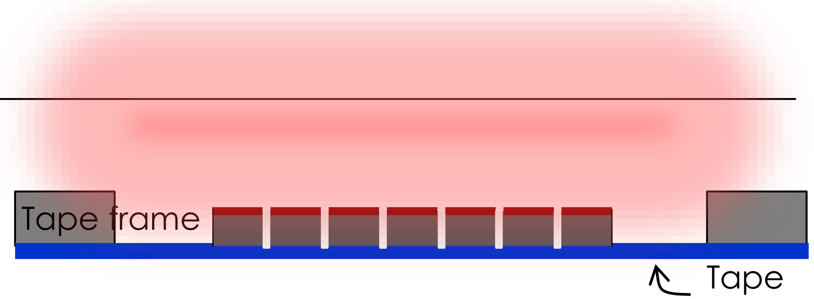
	Blade Dicing	Laser Dicing
Damages	Cracks, chips, debris, water residues	Heat, delamination
Cut speeds	Slow for small dies, thin wafers	Slow for small dies, multiple passes for thicker / multi-material wafers

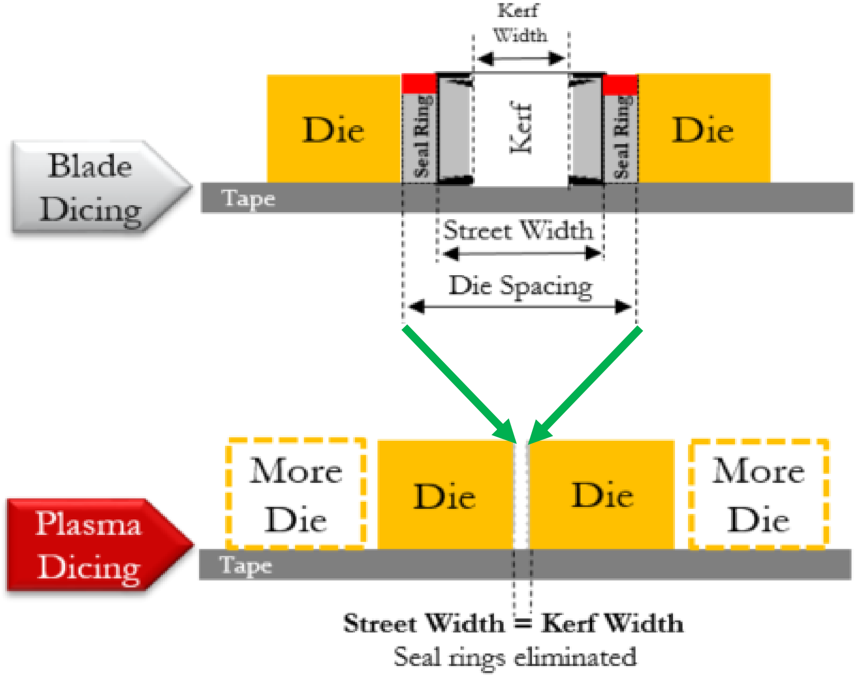


Sequential mechanical / thermal processes limited by beam/ blade dimensions

Parallel + chemical dicing technology: plasma dicing

	Blade Dicing	Plasma Dicing
Street size	> 80 µm	Aspect ratio < 30:1, die picking is usually the bottleneck
Die layout	Orthogonal	No constraint
Damages	Cracks, chips, debris, water residues	Sub-µm sidewall roughness, no chipping, cracking, recast
Cut speeds	Slow for small dies, thin wafers	Slow for thick dies, hard-material wafers
Dimension accuracy	> 10 µm	< 1 µm

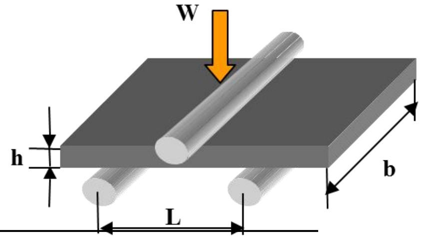


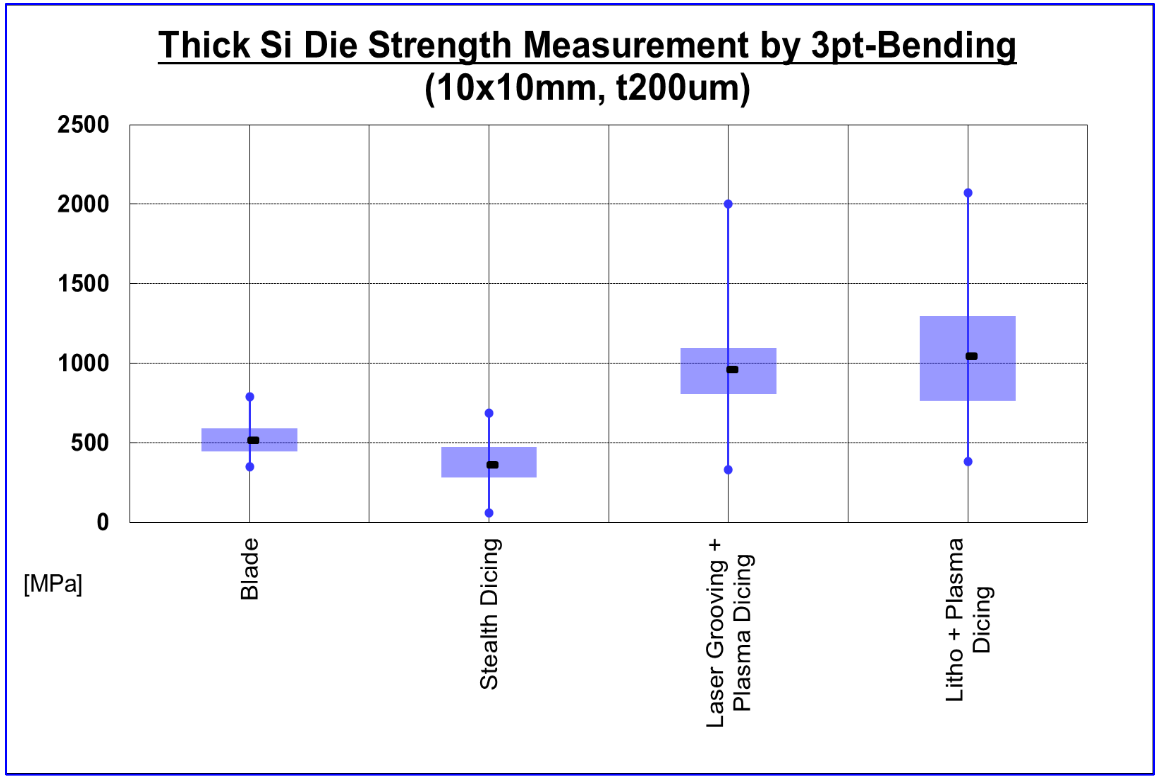


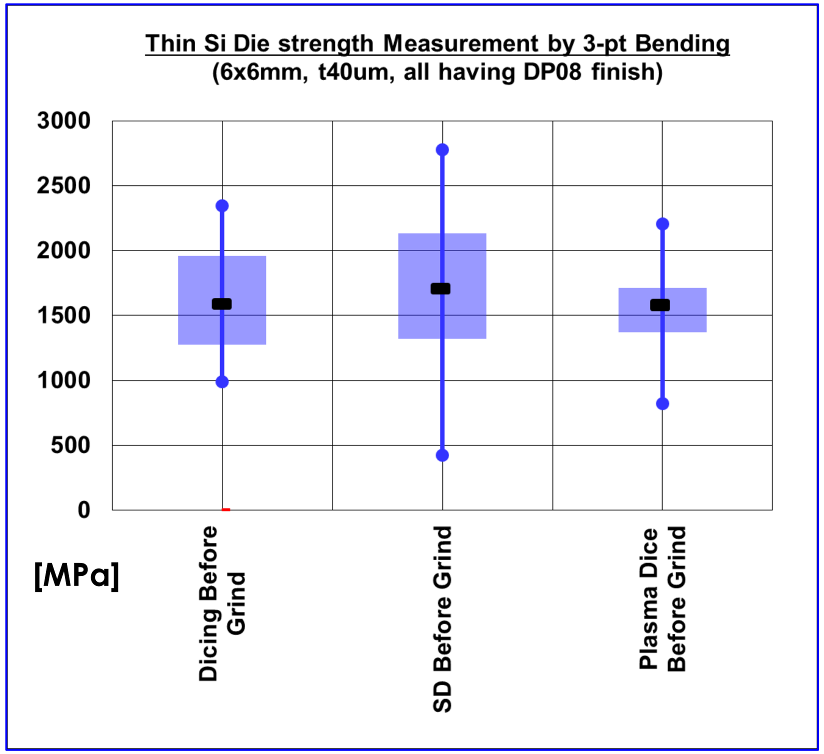
Highest die density and best quality with plasma

Impact on die strength

$$\delta = \frac{3LW}{2bh^2}$$



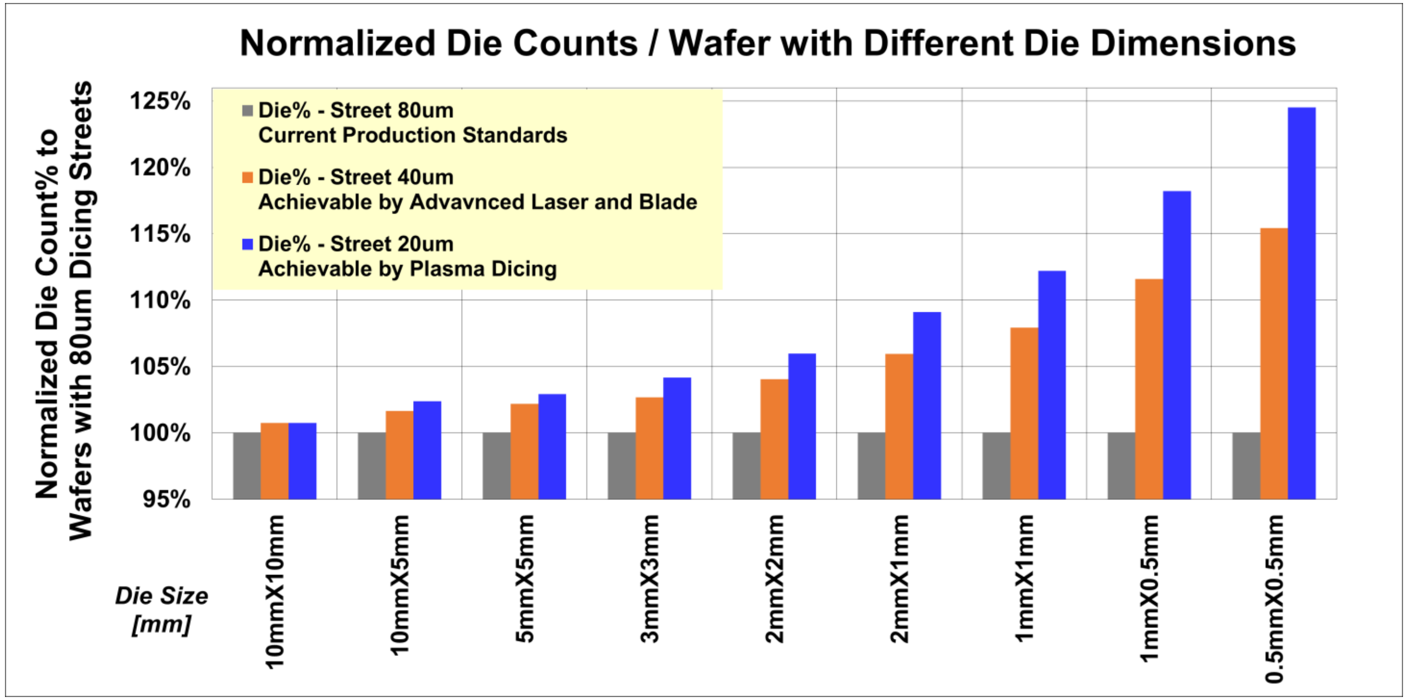

Thick Si Die Strength Measurement by 3pt-Bending (10x10mm, t200um)

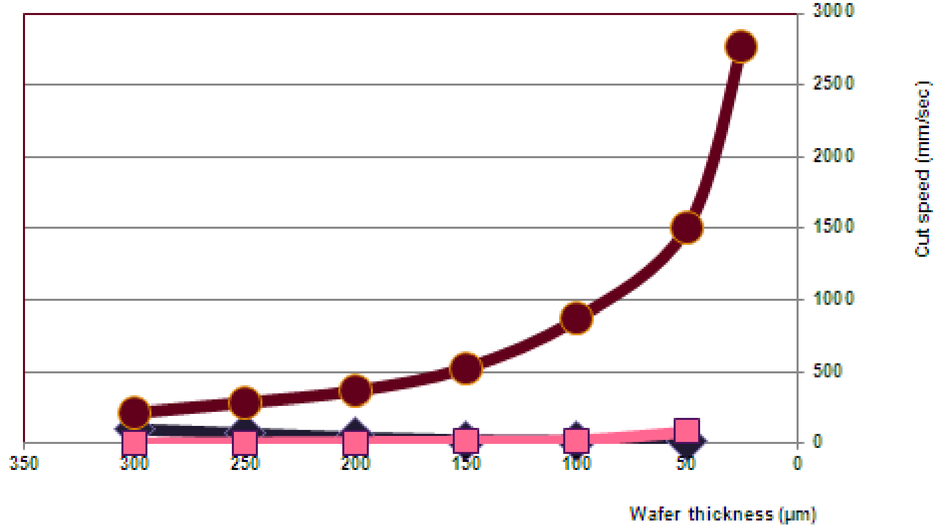

Thin Si Die strength Measurement by 3-pt Bending (6x6mm, t40um, all having DP08 finish)

- Thick die -> sidewall contributions to the die strengths are large
- Sidewall quality correlates to die strengths
- Plasma dicing **improves die strengths** for **thick** dies

- When die is thin, sidewall contributions to die strengths diminishes
- Wafer backside finish quality dominates die strengths
- Same wafer backside finish → **similar thin die strengths**

Impact on throughput

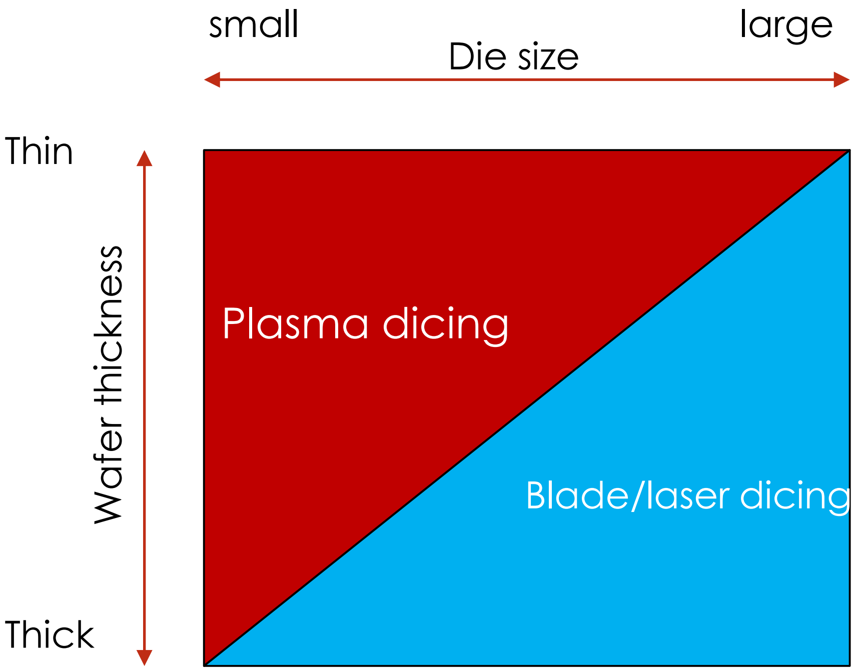




Smaller streets ⇨ More dies
=> higher gains compared to blade dicing

Thinner substrates ⇨ Less to etch
=> Faster cut speed by several order of magnitudes compared to blade dicing.

Throughput and Cost of ownership



Better CoO with plasma dicing for small dies / thin wafers compared to blade dicing

-> complementary approach in terms of CoO.

Even when the CoO is worse with plasma dicing, some applications may need the best quality available.

Plasma Dicing – Integrating FEOL into BEOL

Three-step "Bosch" process

- Passivation ($C_4F_8 \rightarrow (CF_2)_n$)

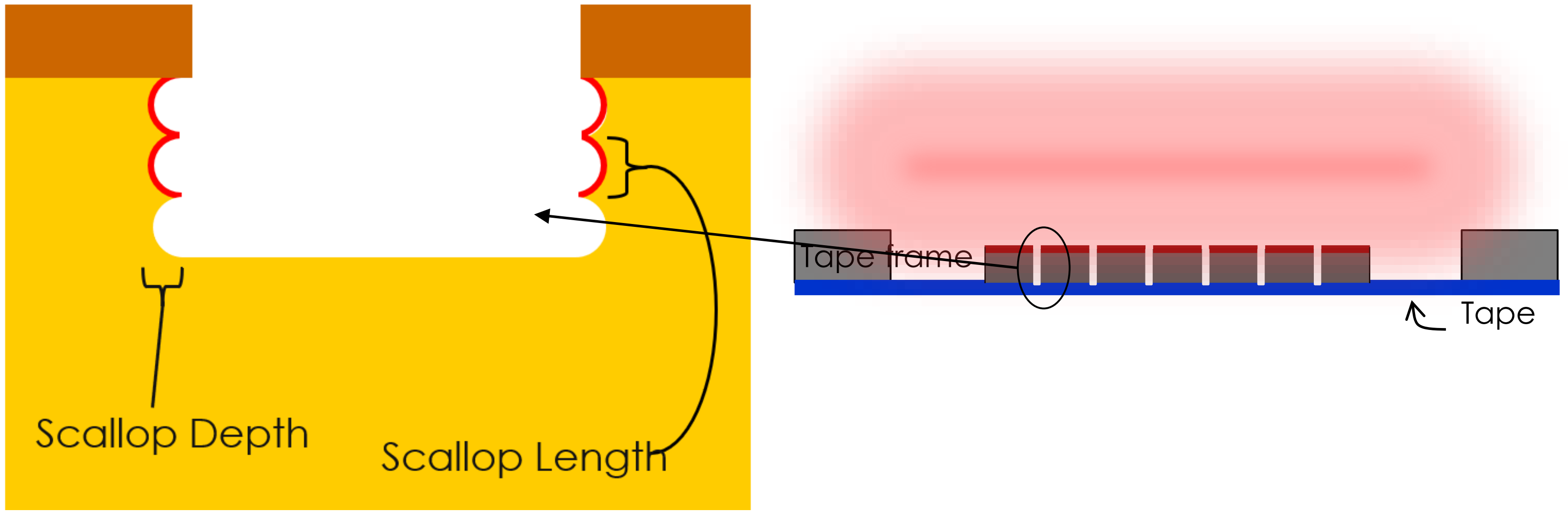
  Deposition

- Selective passivation removal

  Etch A

- Isotropic etching of Si (SF_6)

  Etch B



Most common trade-offs (dicing quality vs throughput) are:
- Large scallop depths vs etch rate
- Large scallop aspect ratio vs selectivity.

Typical performance of plasma dicing processes

Ultra-low damage

Tape temperature is ~60°C (low thermal),
no mechanical action

Materials

High selectivity with SiO2 (1000:1), PR (> 250:1),
possible to etch with metals exposed

Die shapes

Litho-defined

Cut speeds

Typically 25-30 µm / min for Silicon

Dimension accuracy

Litho-defined (~100 nm)

Performance looks promising
(5 min-long process for a common 150 um-thick wafer).
Optional additional mask (SiO/N passivation is enough)

What about the die strength?

1. Limitations of the current dicing technologies and motivations

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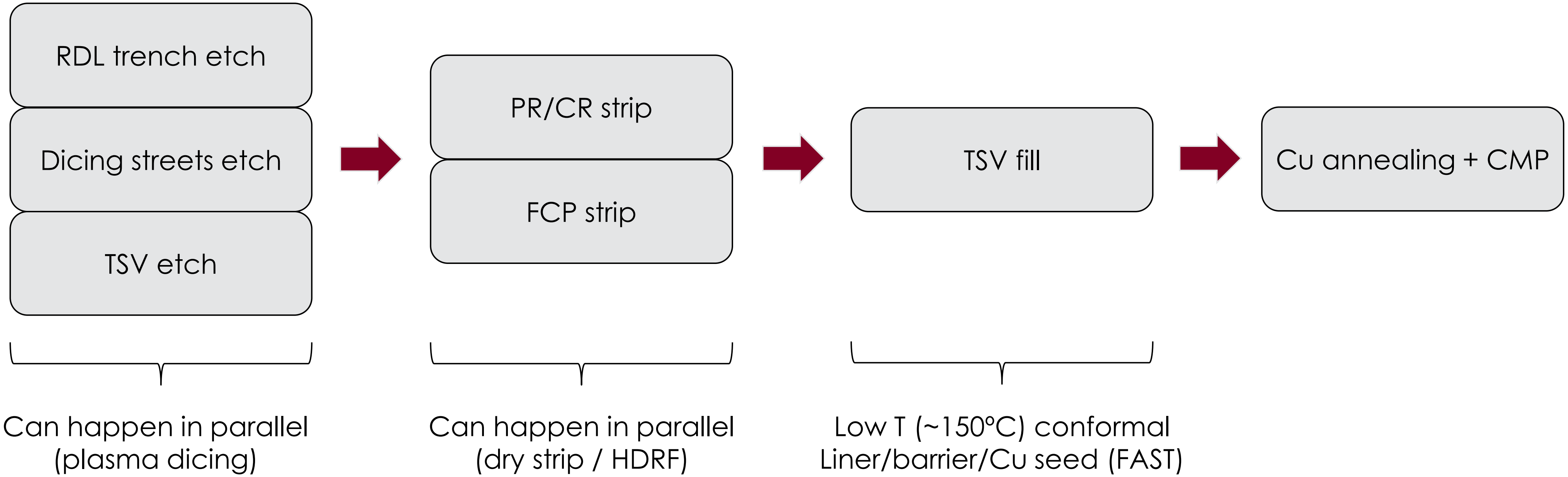
Plasma dicing in a Damascene RDL process flow



RDL trench etch

Dicing streets etch

TSV etch

PR/CR strip

FCP strip

TSV fill

Cu annealing + CMP

Can happen in parallel
(plasma dicing)

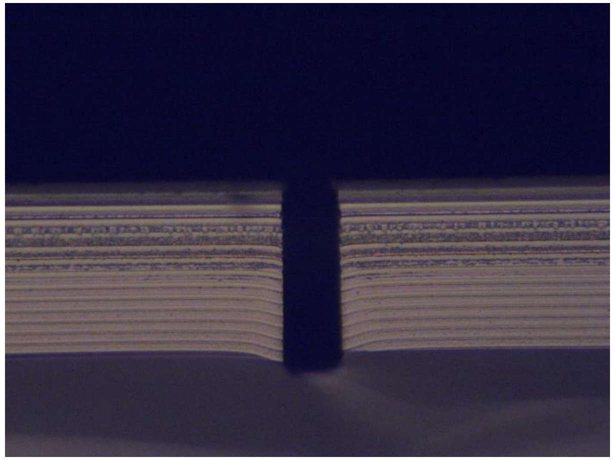
Can happen in parallel
(dry strip / HDRF)

Low T (~150°C) conformal
Liner/barrier/Cu seed (FAST)

Damascene process flow allows higher RDL density, sub-micron L&S.
Plasma dicing and other key technologies allow parallelizing steps.

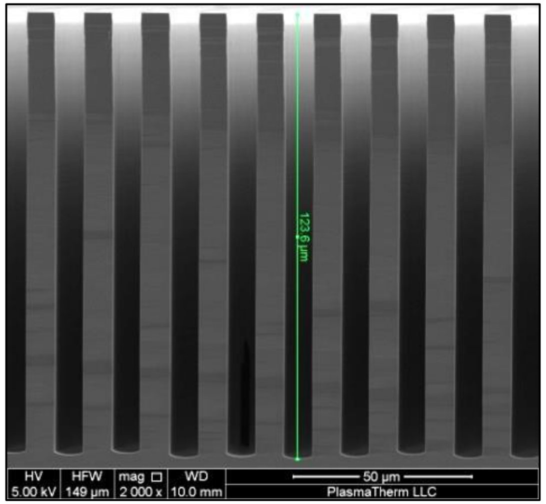
Bonus of plasma dicing – TSV etching during dicing

15µm Trench diameter
400µm deep



High rate

8µm Via diameter
120µm deep

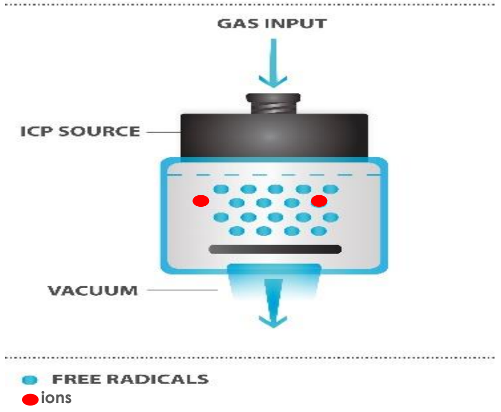


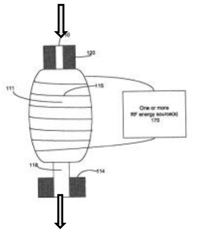
Vertical profile

Fluorocarbon polymer needs to be removed before TSVs can be filled.

HDRF: Efficient fluorocarbon polymer removal

Downstream





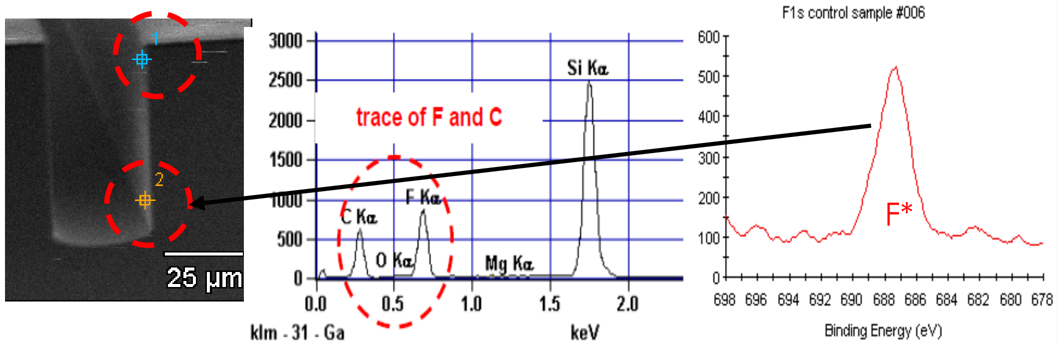
Several small ICP sources

- **High plasma density ICP source**
  - Radicals density > 1E17 cm^{-3}
  - Mainly radicals (~ 10,000 x more than ions at wafer level)
  - Low temperature processing < 70°C
- **Low impact to sensitive devices**

DRIE polymer Via top

EDX analysis

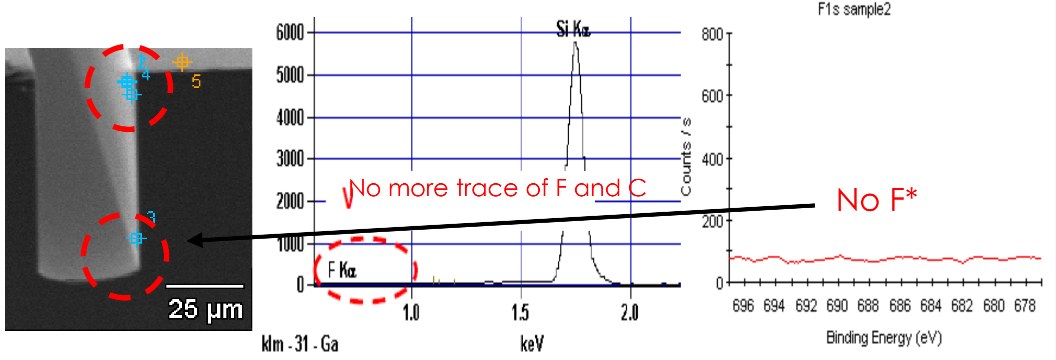
XPS analysis



trace of F and C

F*

After HDRF



No more trace of F and C

No F*

Low Temperature Processes for TSV Integration

Problem:

Scallops

TSV Via Etch

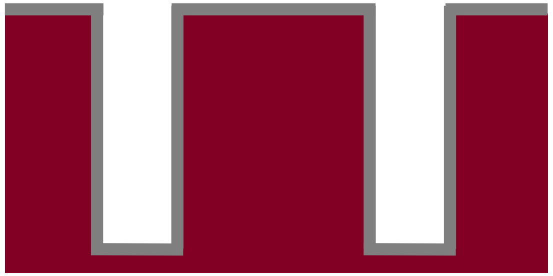
- 10:1 Aspect Ratio
- Smooth sidewalls
- Uniform depth
- Vertical profile
- No undercut

DRIE Si

TSV CVD Liner

- Continuous
- Conformal
- Leakage/breakdown
- Breakdown
- Adhesion
- Thermal budget

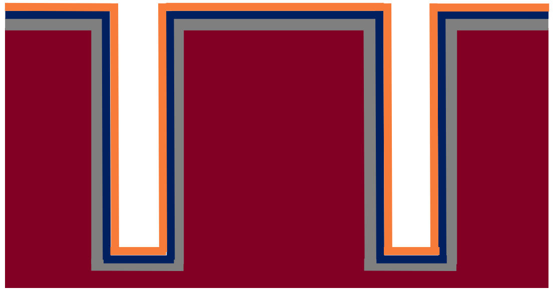
F.A.S.T. SiO_2



TSV Barrier/Seed

- Continuous
- Conformal
- Thermal budget
- Copper compatible
- Low resistivity

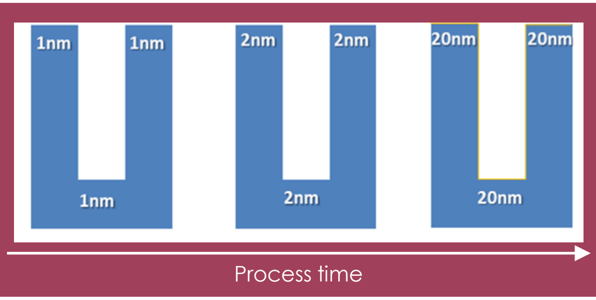
F.A.S.T. TiN/Cu



Plasma-Therm

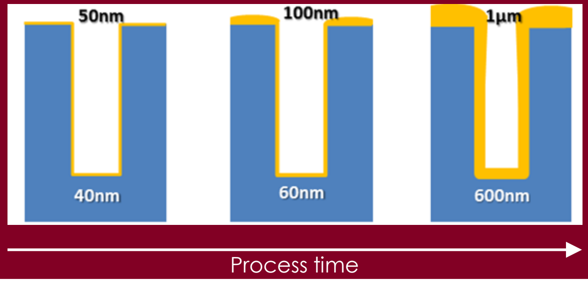
Liner Technology Approaches for TSV

ALD
PEALD



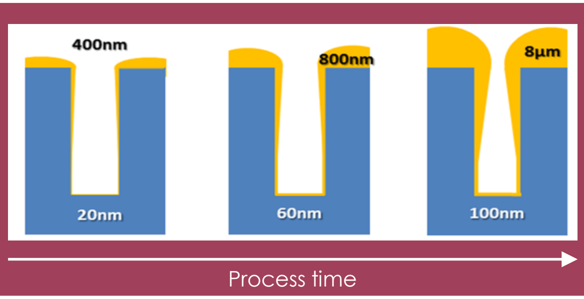
Very thin
Slow rate
Conformal

FAST

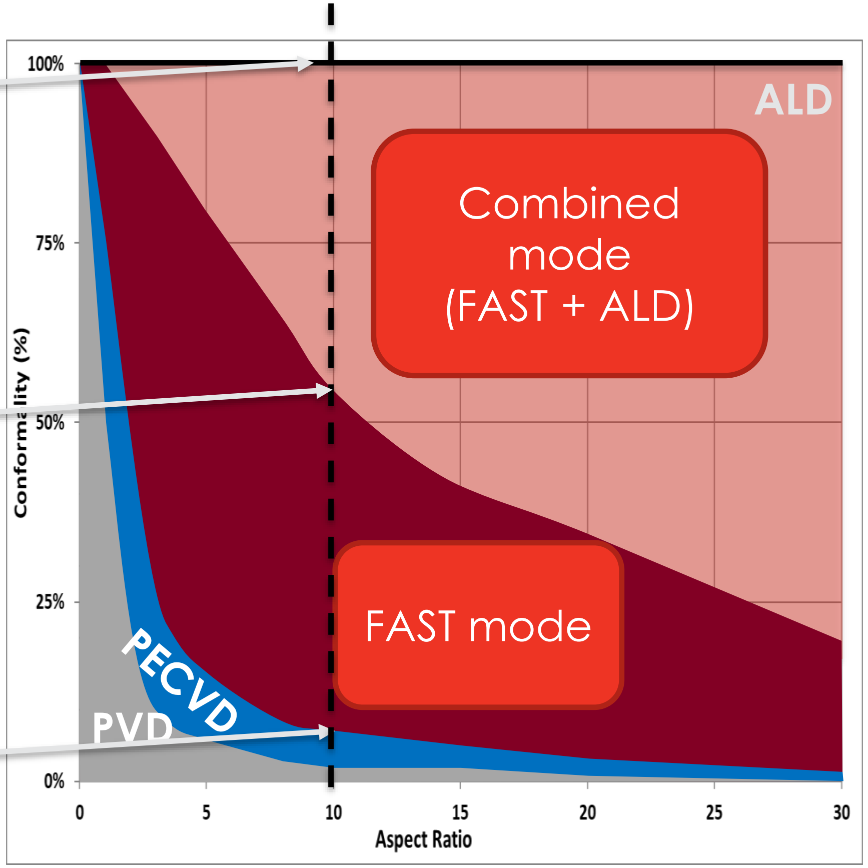


Thick
Moderate rate
Conformal

PECVD



Very thick
High rate
Non-conformal



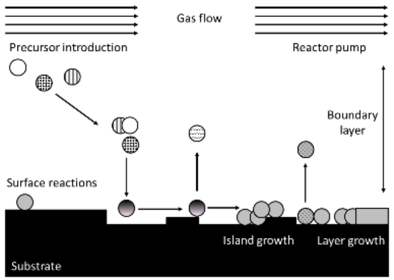
Combined mode
(FAST + ALD)

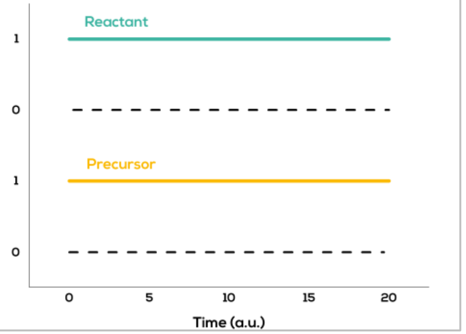
FAST mode

Plasma-Therm

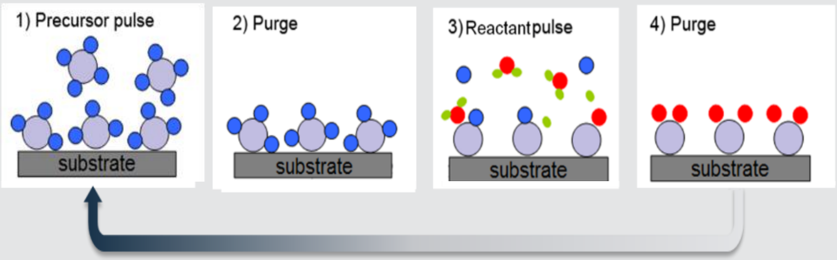
F.A.S.T.® Crossroads of ALD and CVD

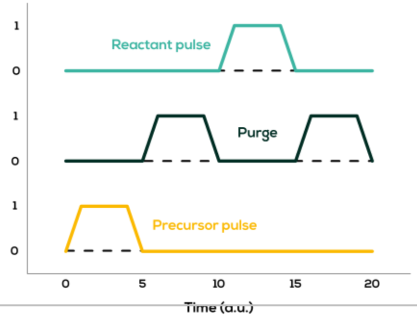
(PE)CVD



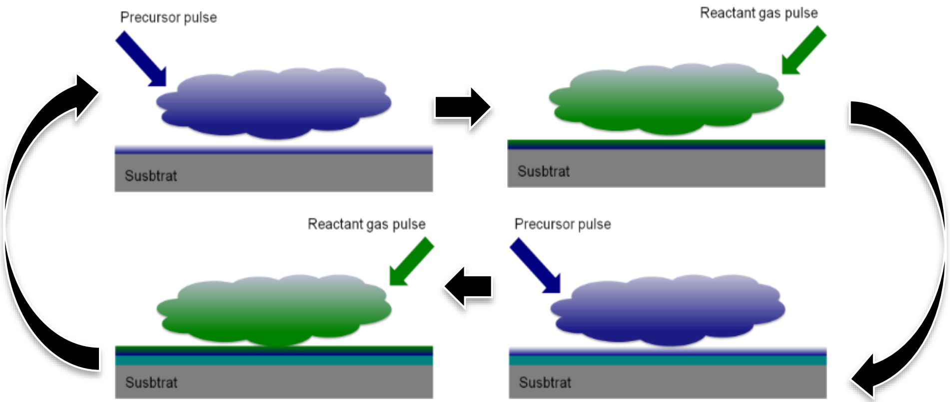


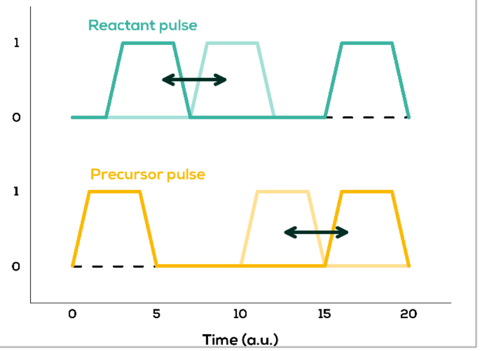
(PE)ALD
Monolayer
growth





Fast
Atomic
Sequential
Technology

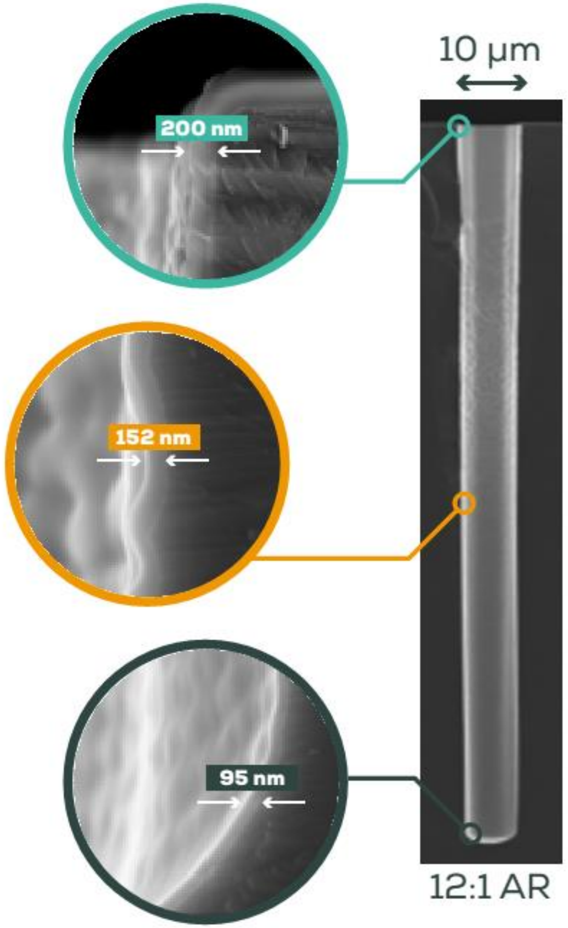


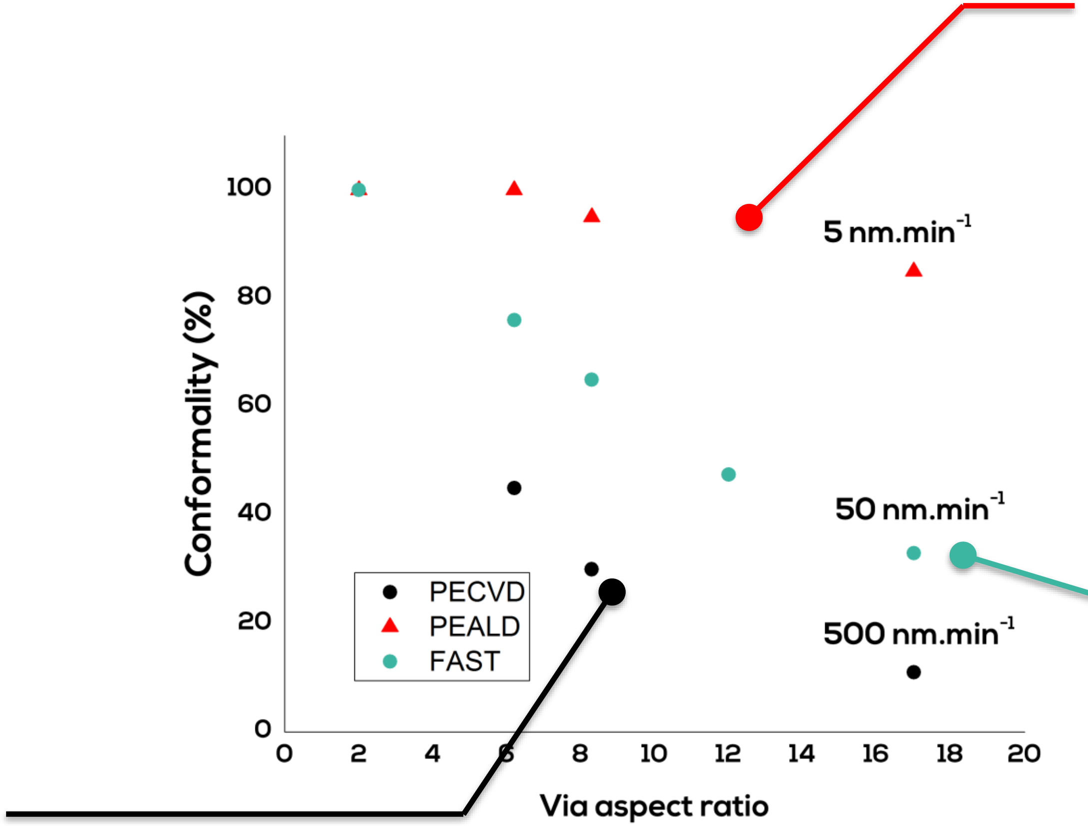


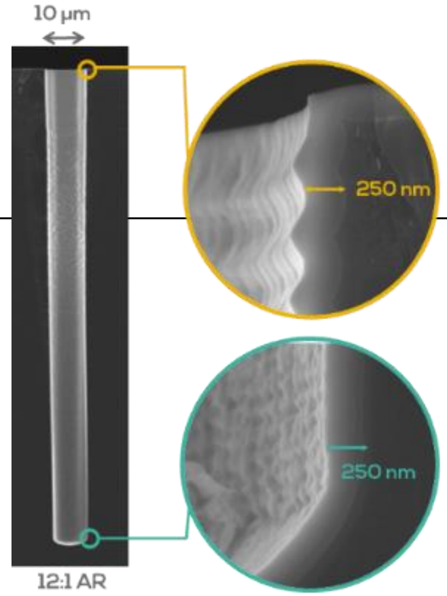
Multilayer growth

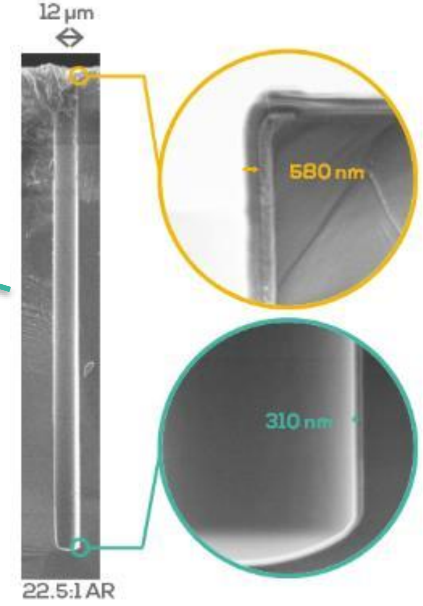
Plasma-Therm

F.A.S.T.® SiO_2 Liner
Conformality adjustable (150°C)



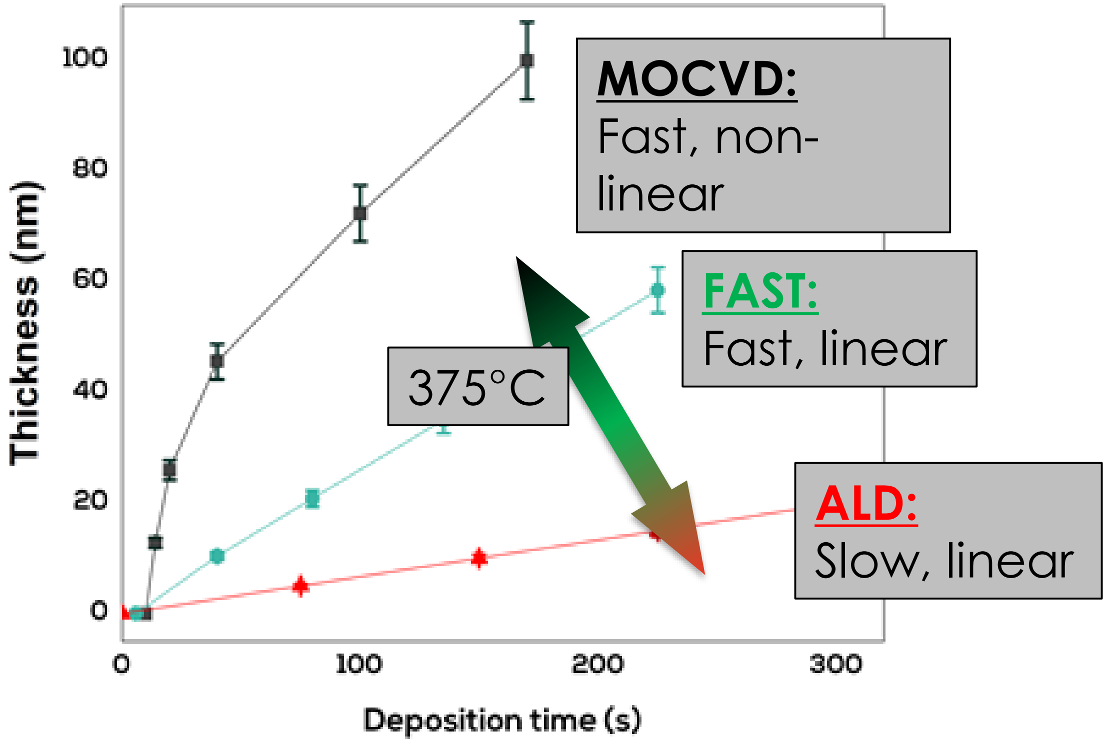






Plasma-Therm

TiN and Cu example with FAST



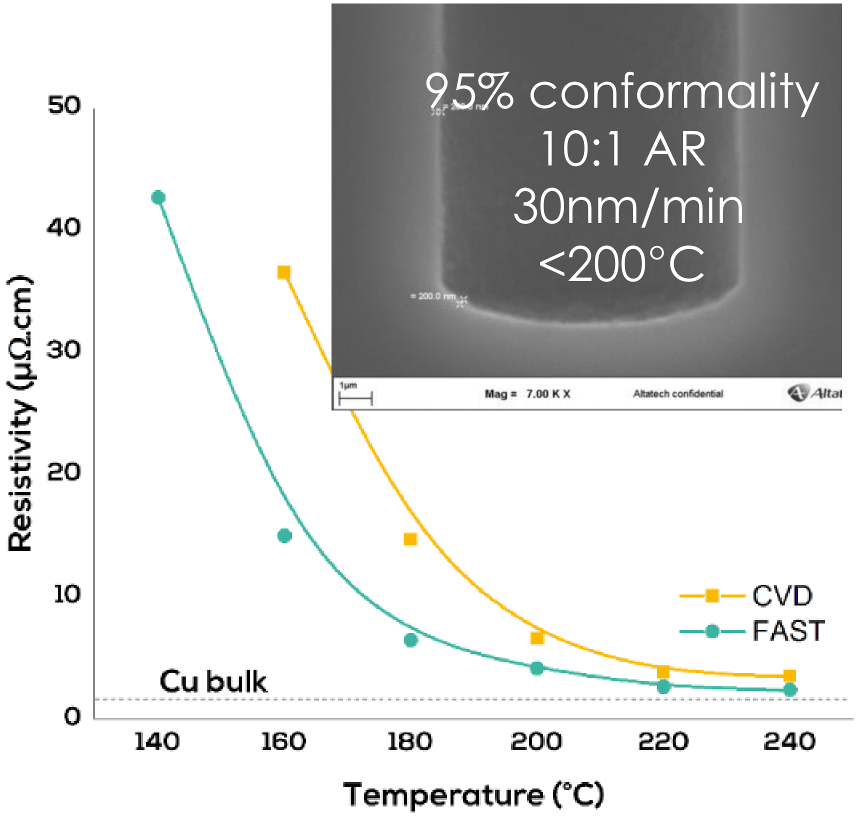
MOCVD:
Fast, non-linear

FAST:
Fast, linear

375°C

ALD:
Slow, linear

TiN



95% conformality
10:1 AR
30nm/min
<200°C

Copper

Conclusion

- Plasma dicing is a complementary technology:
  laser ablation/stealth and saw dicing will not be replaced, only new devices will now be possible.
- Top-notch dicing quality if requirements are extreme.
- 3D/hybrid packaging process flows benefit a lot from plasma dicing.

Thank you for your attention!

ECSEL
Joint Undertaking

VINNOVA

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Surface Activation/Cleaning for Wafer Bonding

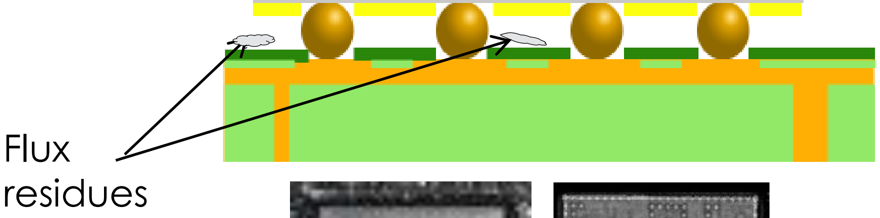
High O* exposure without ions, UV or high temp

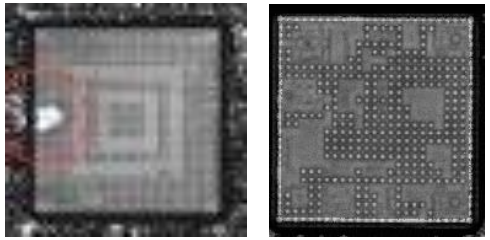
Without plasma treatment

With plasma treatment

Silicon:Silicon
Silicon:Quartz

Improved underfill distribution

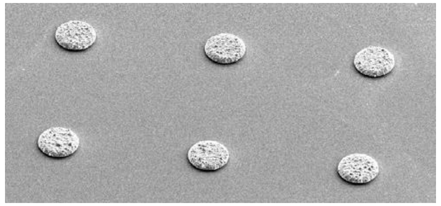


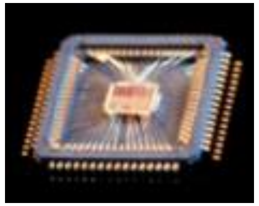


Contact angle 60-80° to 10° with O* radical exposure

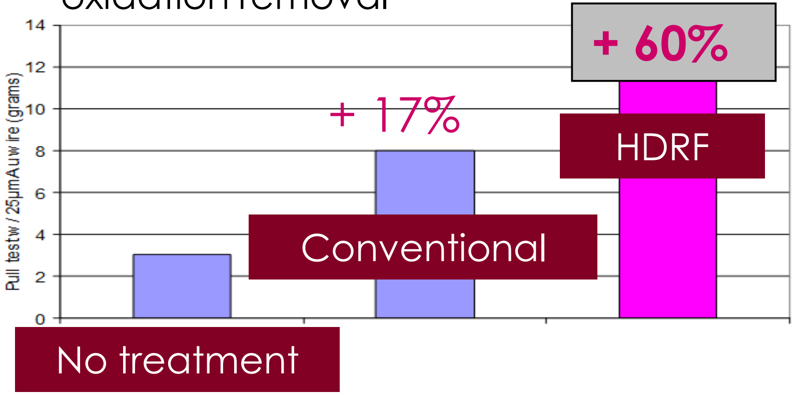
Improved epoxy wetting and void-free reflow

Wire Bonding Pad Cleaning





Contamination and/or oxidation removal



Reduced ion-impact allows longer radicals exposure.
Lower surface activation energy promotes bonding.

Plasma-Therm