Sawing Capability Study for Front Side Chipping Reduction

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Abstract

New wafer technologies characterized by narrower saw street width and presence of complex Test Structures in the area between two dice (Saw Street or Scribe Line) are challenging for wafer sawing in order to achieve a process free of chipping that could penetrate under the groove damaging the active area.

One of the most important problem that affect quality at sawing is the high density of Test Element Group (TEG) made by metal (Al or Cu) in the middle of Scribe Line (SL). These TEGs are the main cause of the blade loading effect during mechanical sawing that consequently lead to a loss of cutting power and a jagged and/or chipped cut.

In this paper it will be presented the activities done on a device technology involving the optimization through mechanical sawing. The methodology used has been selected in order to have the lowest problematic impact for a production plant; it will demonstrate that Z1 cut depth is one of the main variables to take in account for Front Side Chipping reduction.

Key words: blade sawing, chipping/peeling, Z1 cut depth

Introduction

Mechanical wafer sawing is a cutting process in which dice from a wafer are singulated in individual unities. The area that is allowed to be cut during sawing process is called sawing street and the key factor to determine the quality of the process is to value the extent of chipping or peeling since the effect of these phenomena will compromise the function of the device itself or its reliability [1]. Groove is the limit that separates sawing street from device active area. It represents the maximum allowed chipping extension.

TEG structures can be found on the sawing streets and since contain metal (generally Aluminum or Copper) and dielectrics materials (SiO_2) , they are the main cause of chipping and peeling phenomena [1].

The sawing blade is made of an electroplated nickel disc that is the matrix in which abrasive particles are embedded (usually synthetic diamonds) and the cutting power is strictly related to the ability of the blade to expose sharp diamonds on the edges during the cut [2].

Debris generated during the cutting process and especially the metal ones created during the cut of TEGs tend to stick on the cutting blade and accordingly to the literature [2] they are the cause of blade overload. Once the blade is no more able to expose sharp diamonds on its surface, the mechanical effect on the wafer will be silicon micro and macro cracks that will lead to the failure of the device. With the aim of reducing blade overload during, step cut process was introduced and nowadays is widely diffused. In step cut process, two blades named Z1 (thicker blade) and Z2 (thinner blade) works in a synergic way to complete the singulation of the dice of a wafer. In particular, Z1 blade will perform the partial cut removing TEG structures while Z2 will complete the cut sawing up to the dicing tape. The advantage of this technique is that by splitting the process on two blades, it's easier to select a sets of blade Z1/Z2 to increase the cutting quality both for topside chipping reduction (accounted by Z1) and for backside chipping reduction (accounted by Z2). The overall blade loading on each blade will be also decreased [3].

Wafer thickness tolerance is key parameter that affect the real Z1 cutting depth. Cutting machine will cut at a defined cut height set inside the recipe but not depending on the real thickness of the wafer. Consequently the Z1 blade penetration inside wafer will be different.

Grinding process is a step during the wafer fabrication and consist of thinning the wafer to target thickness in order to increase the processability. This step will introduce a wafer thickness tolerance around $\pm 5\%$ of nominal thickness value.

The aim of this work is to analyze the effect of Z1 blade on front side chipping after sawing of TEG structures. In particular, attention is given to the role of Z1 penetration inside the wafer that can be directly correlated to the ability of the blade to "self-sharpen"

during sawing losing the metal particles that cover its surface and cause the overload.

Materials and Method

Structured 8 inch Silicon wafer with 4 Copper metals and Aluminum Cap is used for the evaluation of Z1 cutting depth.

Sawing is performed using dicer equipment in step cut mode after wafer mounting step on dicing tape. Blade used for evaluation have nominal thickness of 40um for Z1 and 30um for Z2.

Z1 cutting depth is the only parameter changed during the evaluation while all the other parameters such as Spindle RPM, Feed Speed and Z2 cutting depth inside the dicing tape are kept constant.

Trials are performed by variating the Z1 height and the associated dimensionless parameter "Partial cut %" defined as:

Partial Cut % =
$$\frac{Z1 \ blade \ penetration}{Wafer \ thickness} \times 100$$

Consequently, an increased Partial Cut % value means deeper Z1 cutting depth.

Cutting quality is then analyzed by performing Visual Inspection (VI) on sawn wafer focusing on front side chipping and peeling of TEGs but also sidewall and backside analysis to investigate if the variation of Z1 cutting depth can induce degradation in these regions.

Results and discussion

Device analyzed shows different TEG structures distributed on wafer scribe lines. Regions where TEG density is higher are more dangerous because the blade loading will be more severe and consequently chipping and peeling phenomena. For this reason, long shaped TEGs will be the once inspected.

Table in Figure 1 represent the list of trials performed in this work:

Trial	Half cut %
1	18.4
2	21.0
3	23.6
4	26.3
5	28.9
6	31.5

Figure 1: List of trials for Z1 cut depth optimization

Frontside Visual Inspection

Trial 1 correspond to the initial situation before optimization where the Z1 cutting depth is the lowest.

Front side visual inspection shows critical TEG chipping with damaged regions touching the

groove or exceeding it. Such situation has to be avoided since it can lead to device failure. An evident representation of this phenomena is shown in Figure 2 where the chipping of a long shaped TEG is shown.



Figure 2: Long shaped TEG structure chipped after sawing. Partial cut % = 18.4

Too shallow Z1 cutting depth on a long shaped TEG affects the loading of the blade edge that is not able to "self-clean" during cutting. Copper and Aluminum residues accumulation reduce the ability of the blade to expose new sharp diamond from the matrix finally causing severe TEG chipping.

Figure 3 shows the results of Trial 3-5-6 where an increased cut depth is performed along the trials.



Figure 3: Long shaped TEG structure chipped after sawing with different Partial cut %

Results shown for Trial 3 on same TEG are similar to Trial 1 with chipping touching the groove. Trial 5 shows an increased cutting quality since chipping phenomena is reduced and no more touching the guard ring. Trial 6 having the highest Z1 cutting depth shows the best results with heavily reduced chipping of TEG as also shown in literature [4].

The increasing of cutting quality with Z1 cutting depth can be associated to the fact that the blade during operation will be able to remove the Copper and Aluminum residues that stick to the blade edges by cutting more silicon below the active area of the die.

Backside & Sidewall Visual Inspection

Backside Visual Inspection has been performed to verify if the variation of Z1 cutting depth can cause a deterioration of cutting quality for Z2 in terms of Backside Chipping (BSC).



Figure 4: Box Plot for Backside chipping comparison between Trial 6 vs. Trial 1

Figure 4 shows the results for Trial 6 vs. Trial 1 in terms of BSC.

The box plot displays no statistical difference between the two trials meaning that an increasing of Z1 cutting depth do not affect the sawing quality of Z2 blade.

This phenomena can be attributed to the fact that while the increasing of cutting depth for Z1 is nearly doubled (passing from 18.1% to 31.5%), the remaining Si cut by the Z2 blade (called Z2 cut %) is still comparable for both the Trials as seen in Figure 5.



Figure 5: Z1/Z2 cutting depth scheme for Trial 1 vs Trial 6

Figure 6 shows the results for Trial 6 vs. Trial 1 in terms of Sidewall Chipping (SC).

Also in this case, the box plot displays no statistical difference between the two trials meaning that sidewall chipping is not affected by Z1 cut depth.



Figure 6: Box Plot for Sidewall chipping comparison between Trial 6 vs. Trial 1



Figure 7: Sidewall Visual Inspection of Trial 1 vs Trial 6

Figure 7 shows the Sidewall VI done on Trial 1 and on Trial 6. Step cut is clearly visible and the effective measured Z1 cut depth results to be lower for both cases respect to the theoretical value and strictly related to the effective wafer thickness post grinding. In particular, Trial 1 shows a Z1 Partial cut % of 12% instead of the theoretical value of 18.4% while for Trial 6 the real value is 24.5% instead of 31.5%.

Conclusions

In this paper, the effect of Z1 blade penetration inside wafer with the aim of reducing front side chipping of TEGs has been analyzed.

From VI of structured wafer front side, we demonstrated that an increase of Z1 cutting depth (expressed as Partial cut %) is able to increase the self-sharpening of the blade due to an increase of the Si portion of the wafer cut by the blade. The increased ability of exposing sharp diamonds allows the blade to maintain its cutting power and not generate micro or macro cracks that lead to the failure of the device.

VI of backside and sidewall shows that an increase of Z1 Partial cut % does not affect the overall quality.

The increased cut depth % is helpful to compensate the thickness tolerance after the grinding step that eventually could cause a too shallow Z1 cut in which the blade is not able to clean the Copper and Aluminum debris and to expose new sharp diamonds.

The analyzed methodology shows that a variation of a non-invasive parameter such as Z1 cutting depth can lead to a big improvement on cutting quality without performing major variation and changes on front end mask set, dicing materials and UPH.

References

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