a HEICO company

3D technology for Advanced Medical Devices Applications

By , Dr Pascal Couderc ,Jerome Noiray,
Dr Christian Val, Dr Nadia Boulay

IMAPS MEDICAL WORKSHOP
DECEMBER 4 & 5,2012

3D Plus
408, rue Hélène Boucher – ZI
Buc Cedex – France
Phone: +33 (0)1 30 83 26 50
www.3d-plus.com

Outline

- Introduction
- Technology of the Stacking of Rebuilt Wafers
- Medical Applications
- Conclusions

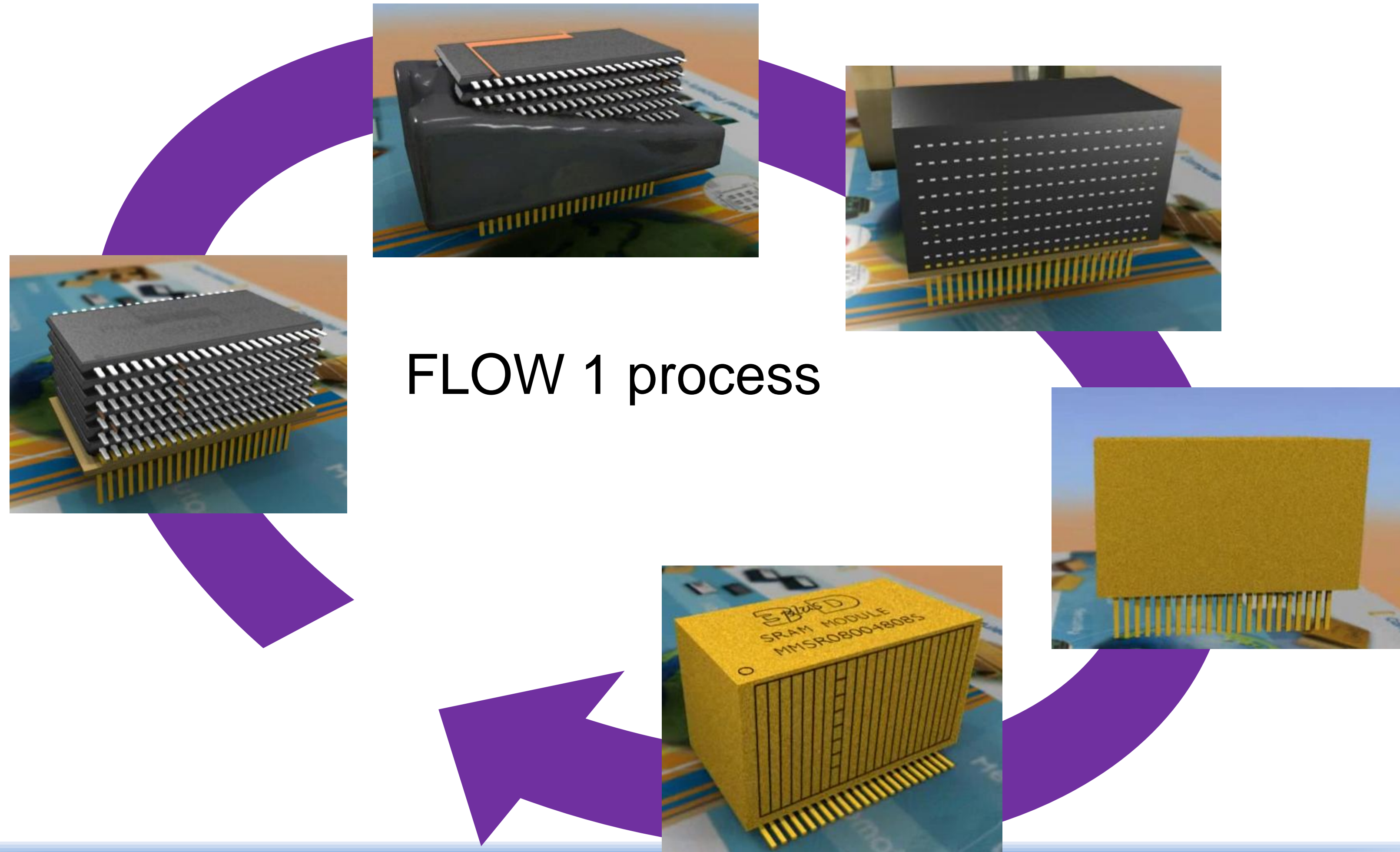
Outline

- Introduction
- Technology of the Stacking of Rebuilt Wafers
- Medical Applications
- Conclusions

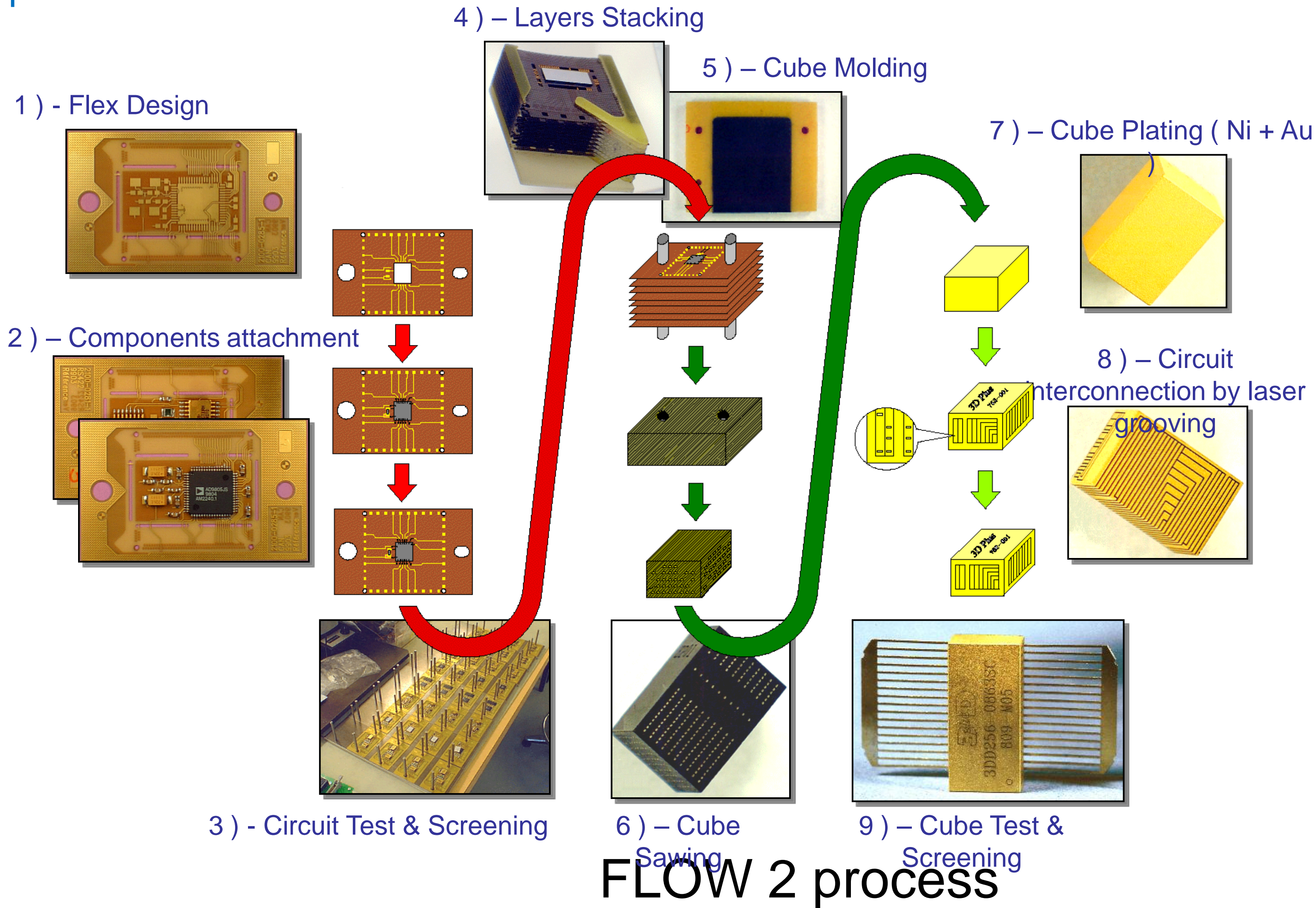
Introduction

- Spin off from Thales (1996)
- From September 2011, 3D-Plus is a 100% subsidiary of HEICO company
- Strong R&D from the 3D Plus launching
- Active patenting policy
- Space certifications from CNES, ESA, NASA, JPL,JAXA, CAST etc…
- ISO 9001 from 2003
- Exportation: 90%
- Workforce : 110
- R&D : 11 including 5 PhD

- 3D-Plus is leader in space 3D memories stacking



Introduction



FLOW 2 process

Introduction

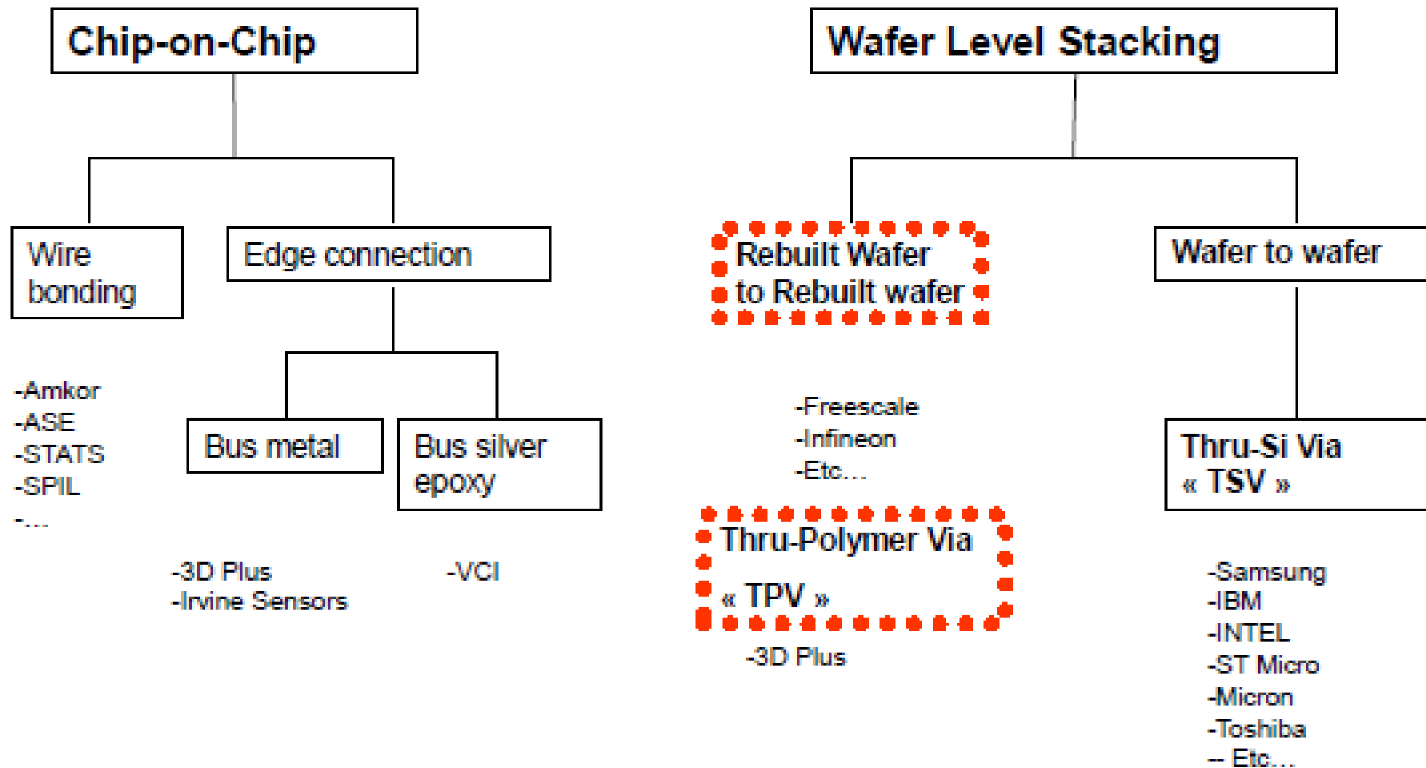
FLOW 2 process: Xray picture

3plusD
a HEICO company

Outline

- Introduction
- Technology of the Stacking of Rebuilt Wafers
- Medical Applications
- Conclusions

3D Existing Packaging Technology



Limits of Wafer to Wafer with TSV

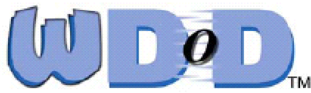
- Non multi sourcing wafers
- Need for smallest possible Via (2µm Ø, leads to a thickness of 20 µm or less ➔Yield of these filled via is low (redondancy is needed)
- Difficulties with SiP, since dies of different sizes
- TSV stresses (keep out zone between 20 to 200 µm)
- Unfortunately impossible to have 100% good wafer ➔ very low global yield

WDoD ™(1) initial criteria

- Use of multi sourcing wafers
- Stacking of 10 levels per mm, now
- 20 levels/mm in development
- Size: 100µm around the larger Die
- Stacking of Known Good Rebuilt Wafer (KGRW)
- Possibility to stack Known Good Burn-In Rebuilt Wafer
- Parallel processing/Panelization from A to Z

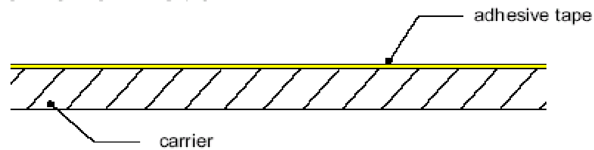
(1) Wirefree Die on Die – Trade Mark from 3D Plus

Technology of the Stacking of Rebuilt Wafers

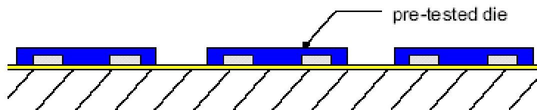


FLOW 3 **" WDoD"**

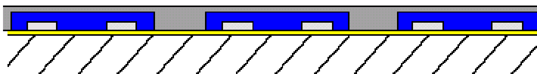
1 - Carrier lamination



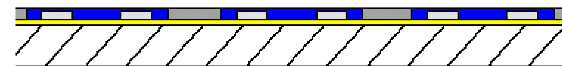
2 - Pick, Flip and place / Die on tape



3 - Compression Molding / Panel encapsulation

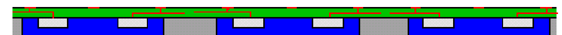


4 - Grinding (optional)

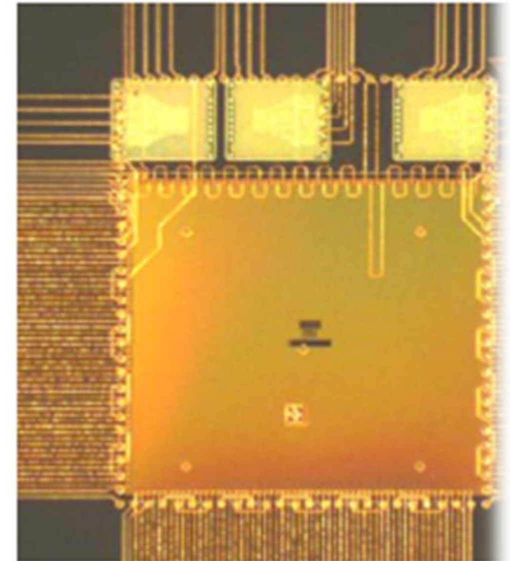


5 - De-taping

6 - Redistribution layer "RDL"

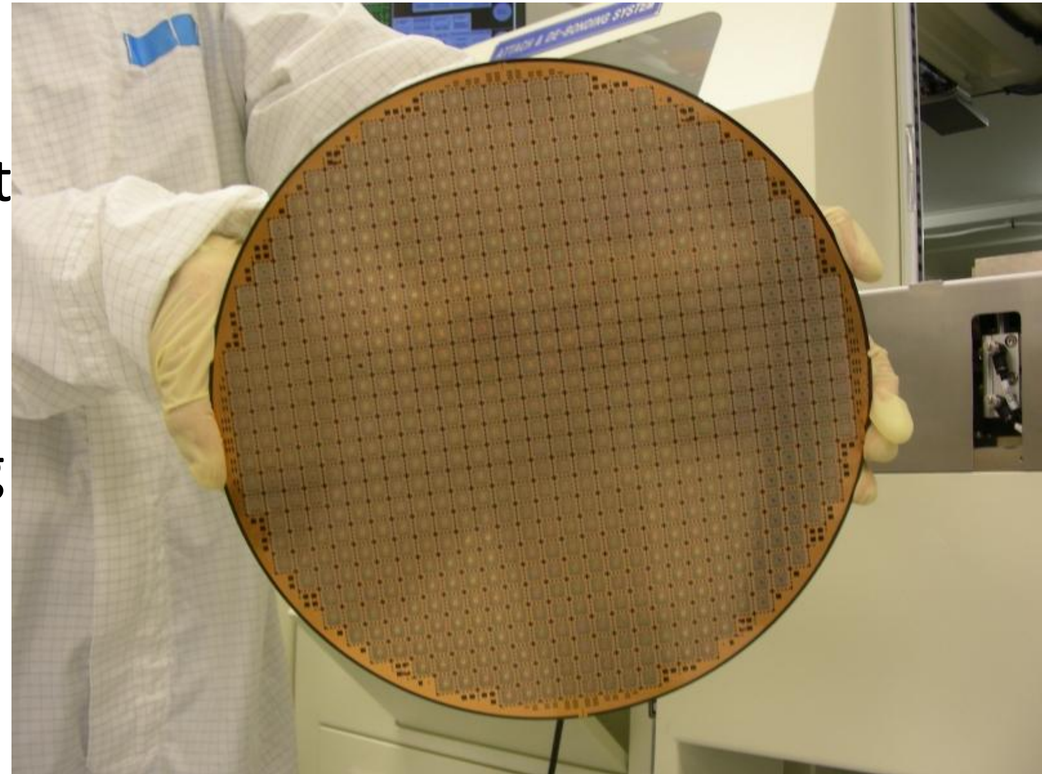


Technology of the Stacking of Rebuilt Wafers



Redistributed Chip Package

- Ultra Low k Compatible
- Good Thermal Management
- No package substrate
- No wire bond / bumps
- Large Area Batch Processing
- Single Chip or Multi Chip
- Improved Integration
- 3-D IC Enabling
- Embedded Passives, Antennas, MEMS



300 mm round panel
9 x 9 mm packages
258 IO, 0.5 mm pitch
716 packages/panel
2 layer build-up

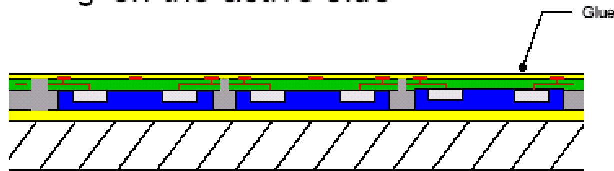
Technology of the Stacking of Rebuilt Wafers

3DplusD a HEICO company

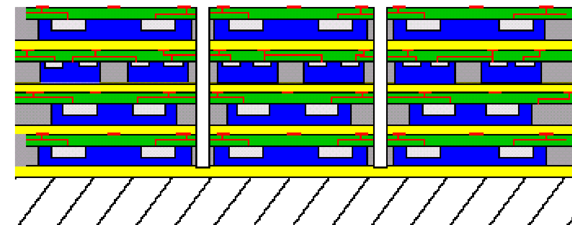
WDoD™

FLOW 3 " WDoD"

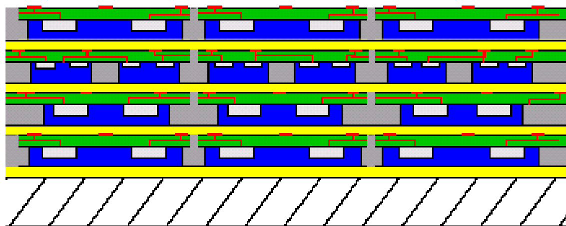
7 - Gluing on the active side



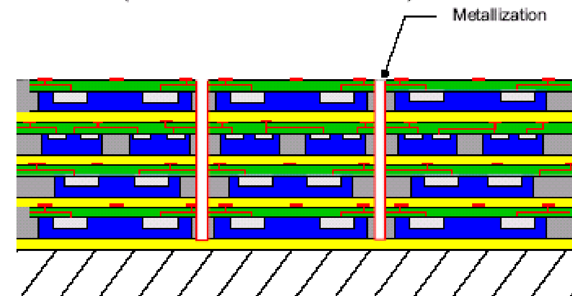
9 - Dicing of the rebuilt and stacked wafers



8 - Stacking of the "Known Good Rebuilt Wafer"



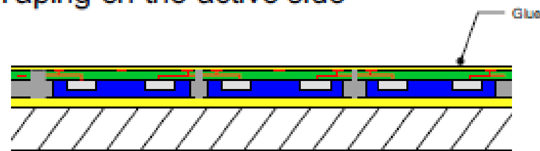
10 - Dicing street edges plating parallel process (electroless Ni + Au)



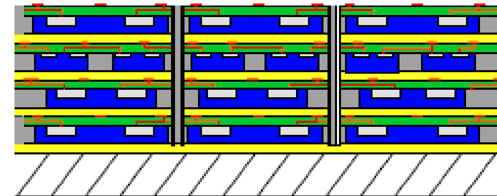
Technology of the Stacking of Rebuilt Wafers

FLOW 3 **" WDoD" with TPV**

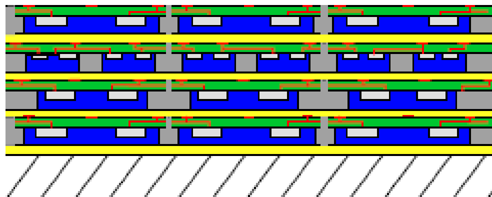
7 - Taping on the active side



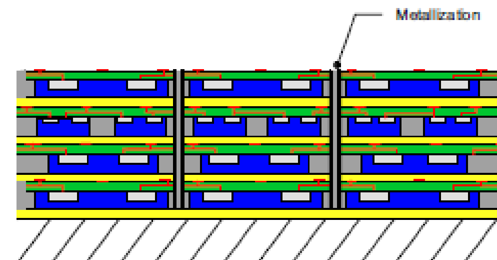
9' - Thru - Polymer - Via "TPV"



8 - Stacking of the "Known Good Rebuilt Wafer"



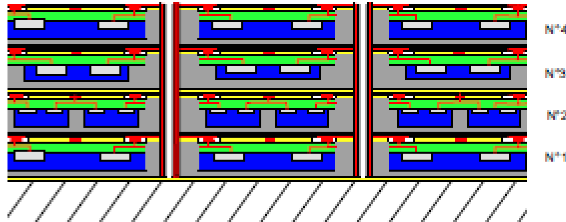
10' - Plating - "TPV"



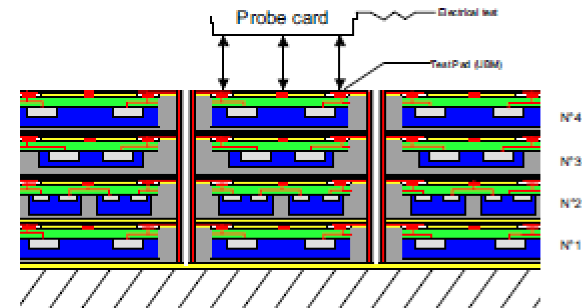
Technology of the Stacking of Rebuilt Wafers

FLOW 3 " WDoD" with TPV

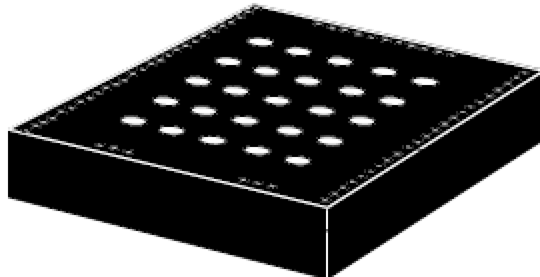
11' - Dicing of the rebuilt and stacked wafers



12' - Electrical test at the wafer level
(Before singulation)

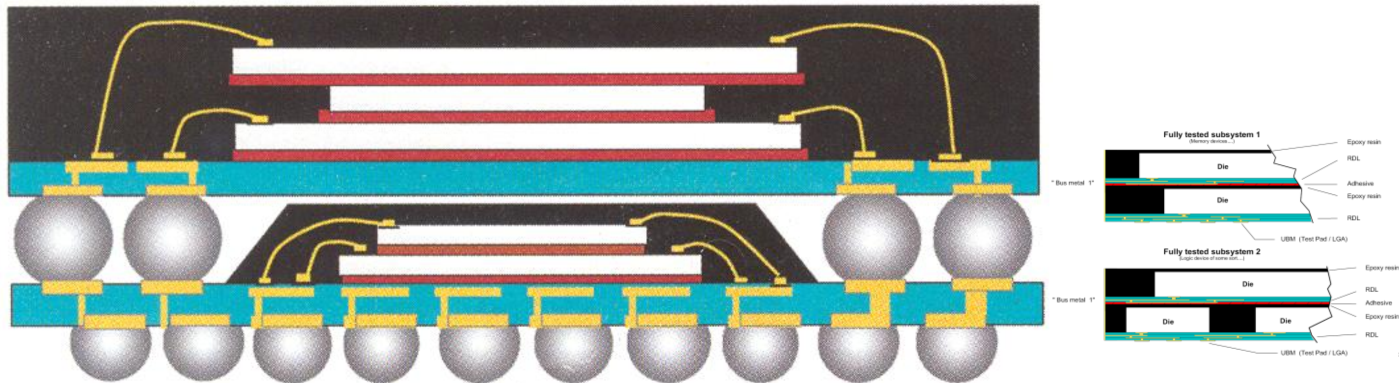


13 - Singulation



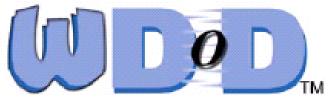
3200-2607-1

Technology of the Stacking of Rebuilt Wafers



PoP and WDoD package relative dimensions

Technology of the Stacking of Rebuilt Wafers



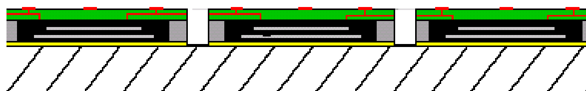
FLOW 3 " WDoD"

OPTION 2
(SiP/PoP with burn-in Subsystems)

7'' - Electroless Ni/Au "UBM" of the subsystem
On 2 stacked Rebuilt Wafers

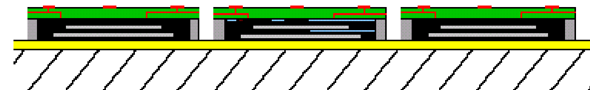
8" - Taping

9" - Dicing

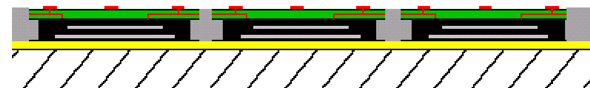


10" - Electrical tests / Burned-in
On 2 stacked Rebuilt Wafers

11" - Pick,Flip and place / Known Good Rebuilt Subsystem on tape

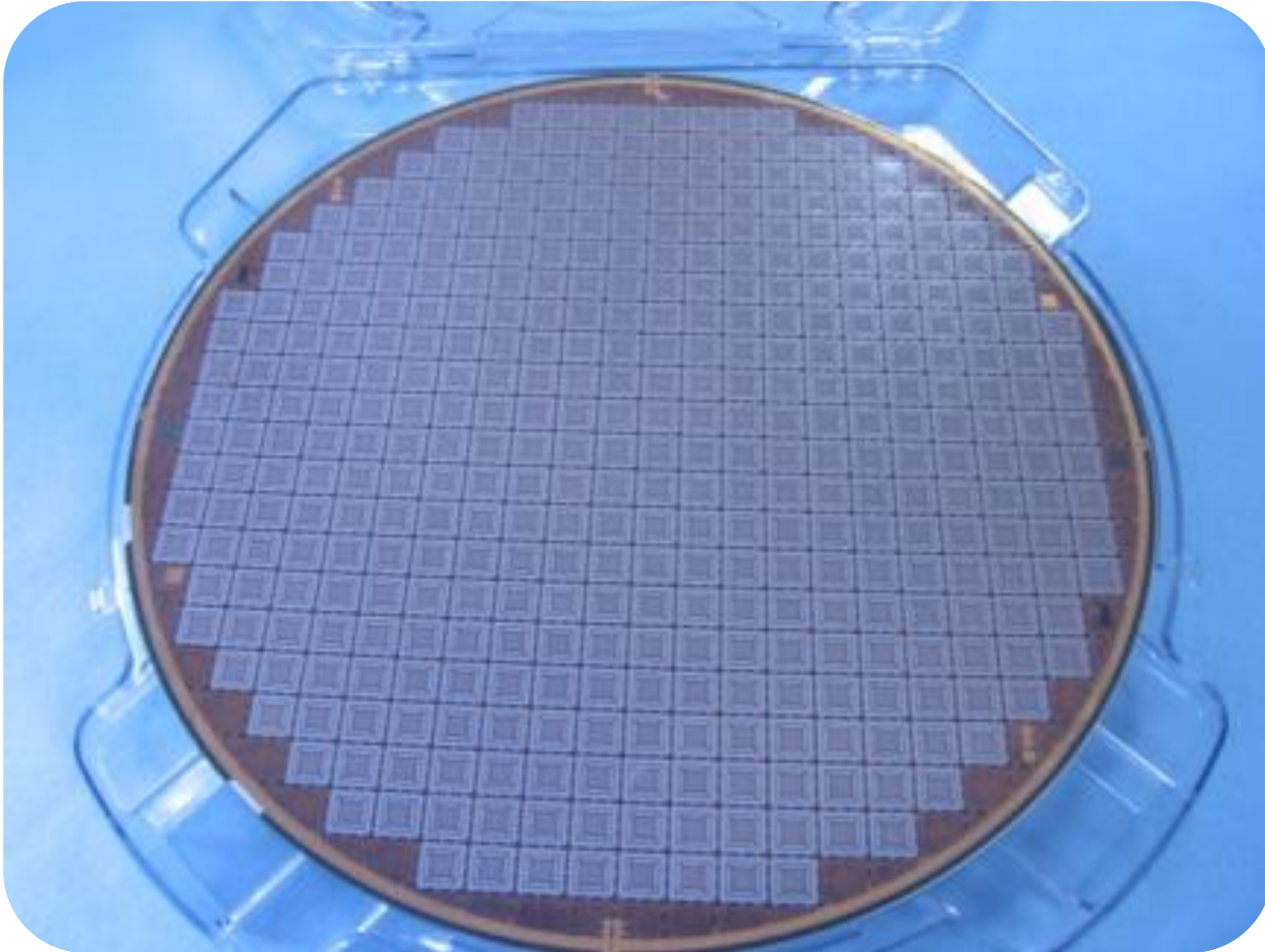


12" - Compression Molding / Curing
(Known Good Subsystem Rebuilt Wafer)



Steps 7 to 12 : Depending on the electrical tests coverage and / or the burn-in

Technology of the Stacking of Rebuilt Wafers



3D plus
a HEICO company

Technology of the Stacking of Rebuilt Wafers

COMPARISON BETWEEN WAFER LEVEL PACKAGE WITH TSV, WITHOUT TSV AND PoP TECHNOLOGIES

	PoP	WAFER LEVEL PACKAGE	
		Wafer to Wafer with TSV	Rebuilt Wafer to Rebuilt Wafer without TSV
Stacking of different size of the die			
More than 1 Die/Level			
Sourcing flexibility			
Test and / or burned-in before stacking			
Package size			
Package height			
Cost			

Best

Good

OK

Poor

Outline

- Introduction
- Technology of the Stacking of Rebuilt Wafers
- Medical Applications
- Conclusions

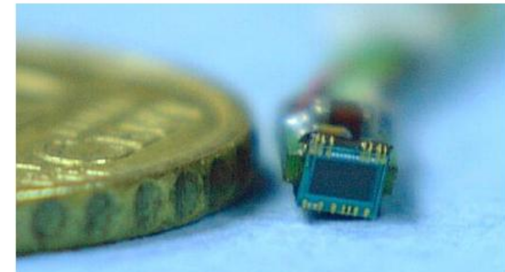
MEDICAL APPLICATIONS:

- Micro camera for Endoscopy (1,5 x 1,5 mm)
- Hearing aids
- Modules for Pacemaker, Neuro stimulator
- Module for 40 silicon capacitors on 20 levels
- US sensor
- X Ray sensor

Medical Applications (1)

Color CMOS Micro Camera Head
SMMC13039

General Description:



The new **3D Plus** Micro Camera is a highly miniaturized, light weight, high performance and easy-to-use colour CMOS Camera.

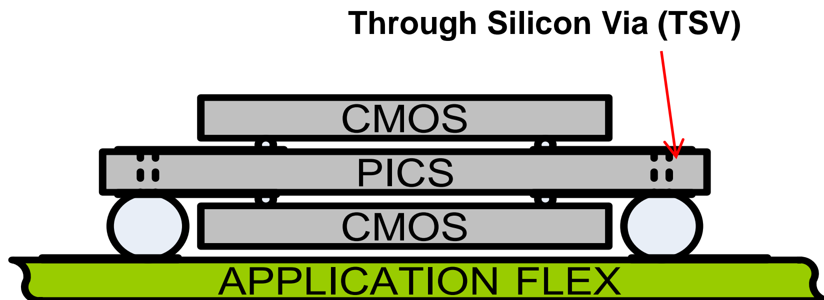
It embeds a CMOS digital sensor with transceivers and decoupling capacitors. The sensor is a 1/13 inch CMOS digital image sensor with an active array of 648 x 488 pixels. It includes sophisticated camera functions such as auto exposure control, auto white balance, black level control, flicker detection and avoidance and defect correction. The decoupling capacitors and transceivers grant it to drive a long length cable directly from the chip. It is designed for low light performance and programmable through a simple serial interface.

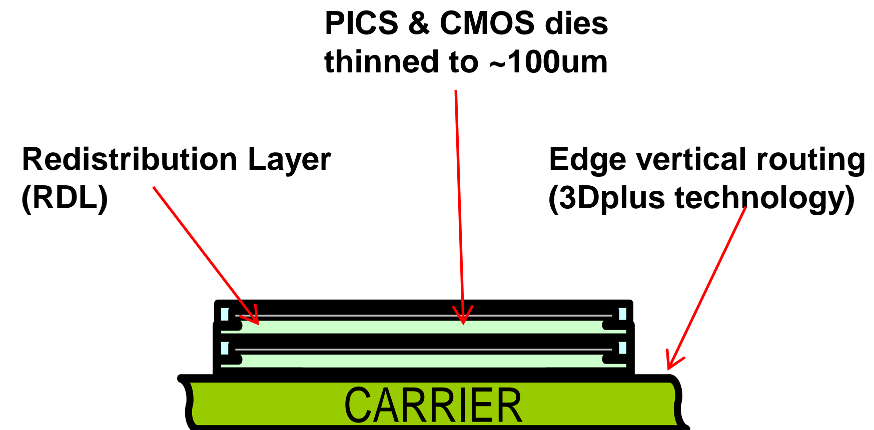
The new **3D Plus** Micro Camera fits very well applications requiring long length cable driving capabilities such as endoscopes. The innovative design makes them also suitable for applications in the area of robotics, assembly and mounting devices or manipulators.

Medical Applications (2)

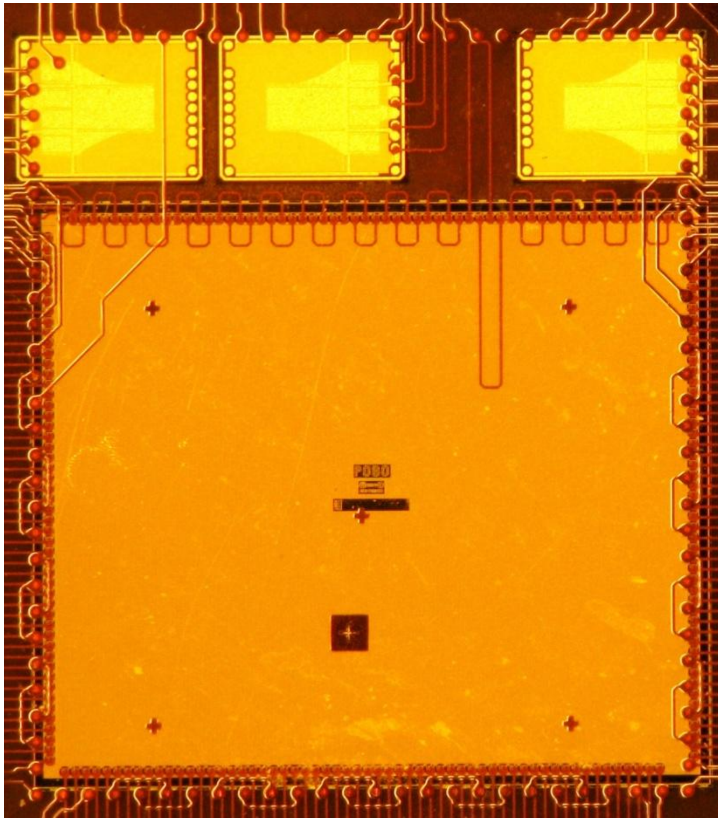
HEARING AIDS

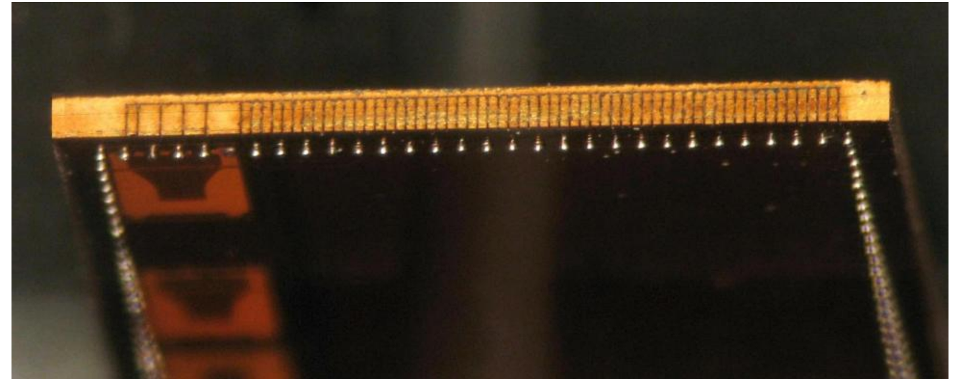
- **Going further than flip-chip – 3D SiP integration for hearing aids**
  - Through Silicon Vias (TSV)
  - Edge Vertical Routing (Based on 3DPlus technology)





Medical Applications (3)





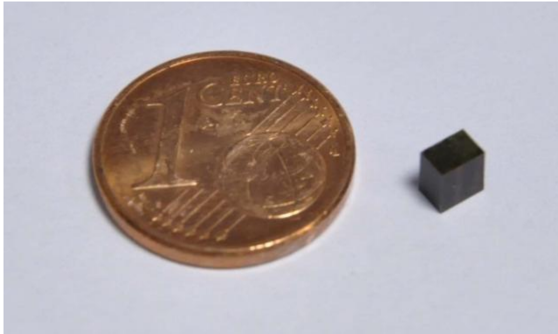
Demonstrator with PICS and DS die for qualification with one major pacemaker manufacturer

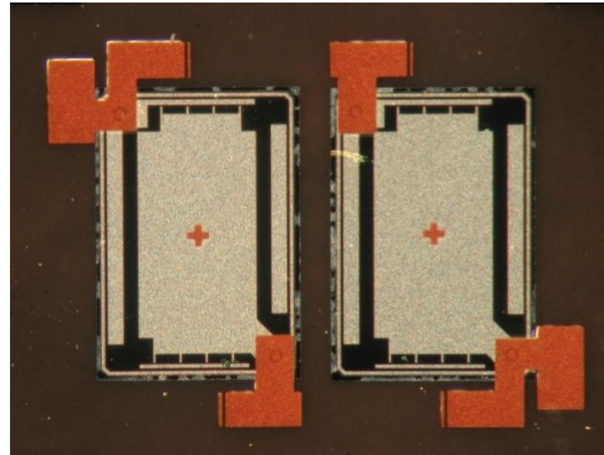
Medical Applications (4)

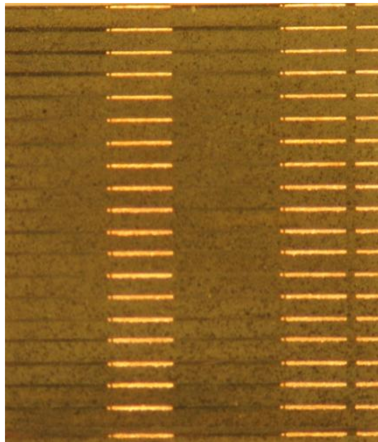
Neurostimulator:

-Diameter 3 mm
-1 MEMS
-3 ASICs
-1 analogic die
-2 capacitors
-1 antenna

Medical Applications (5)

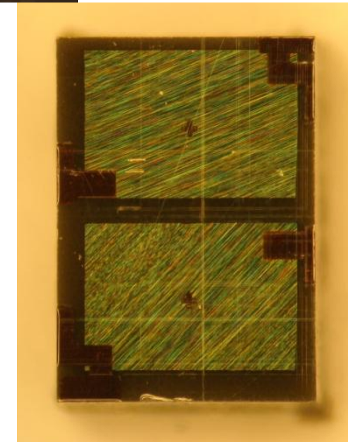




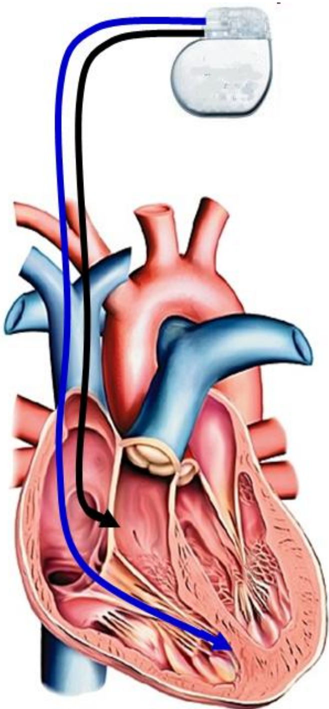


PICS capacitors stack

-20 levels of capacitors pairs

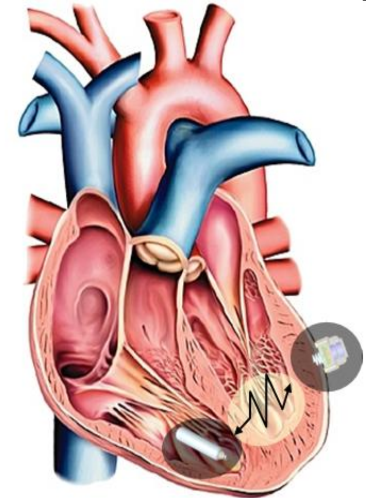


LEADLESS PACEMAKER DEMONSTRATOR IN FP7 PROGRAM:



Objectives

- Realization of a "leadless" pacemaker demonstrator
  - Reduce the size by x 16 (8 cc → 0.5 cc)
  - Eliminate the connecting leads

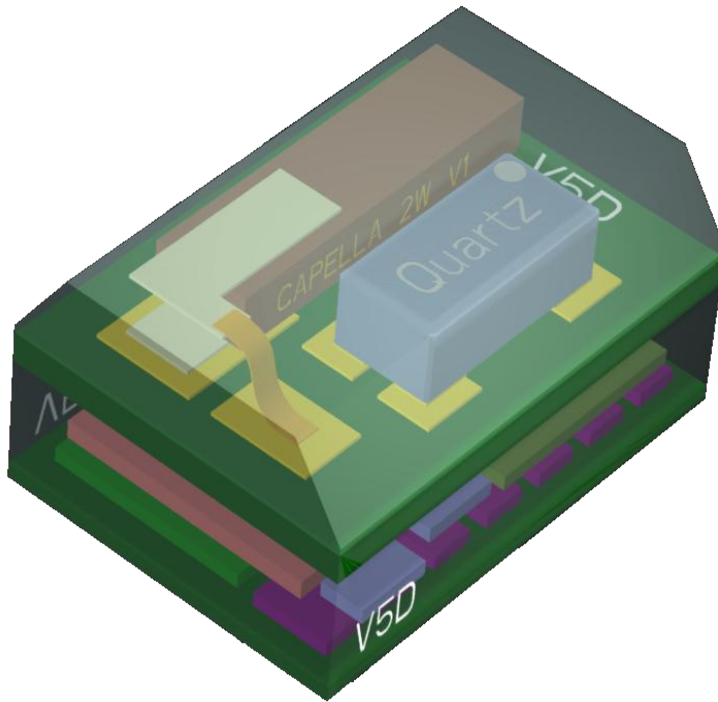


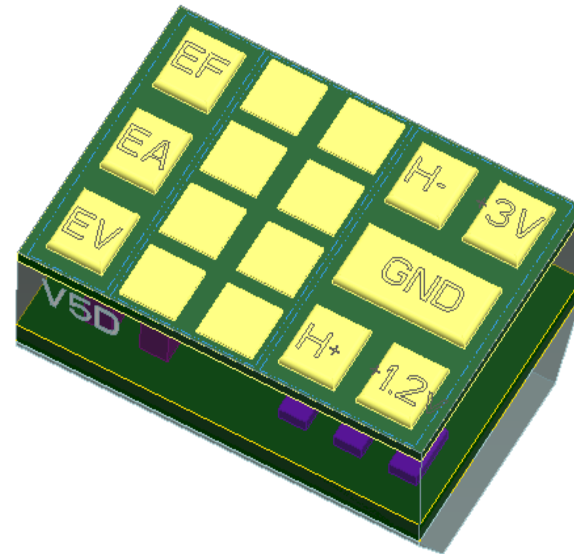
Medical Applications (6)

- Energy scavenger : heart contraction movement → electrical energy
- Low Voltage ASIC
- High Voltage ASIC
- High density isolated capacitors : power storage
- Assembly of electronic in 3D stacking

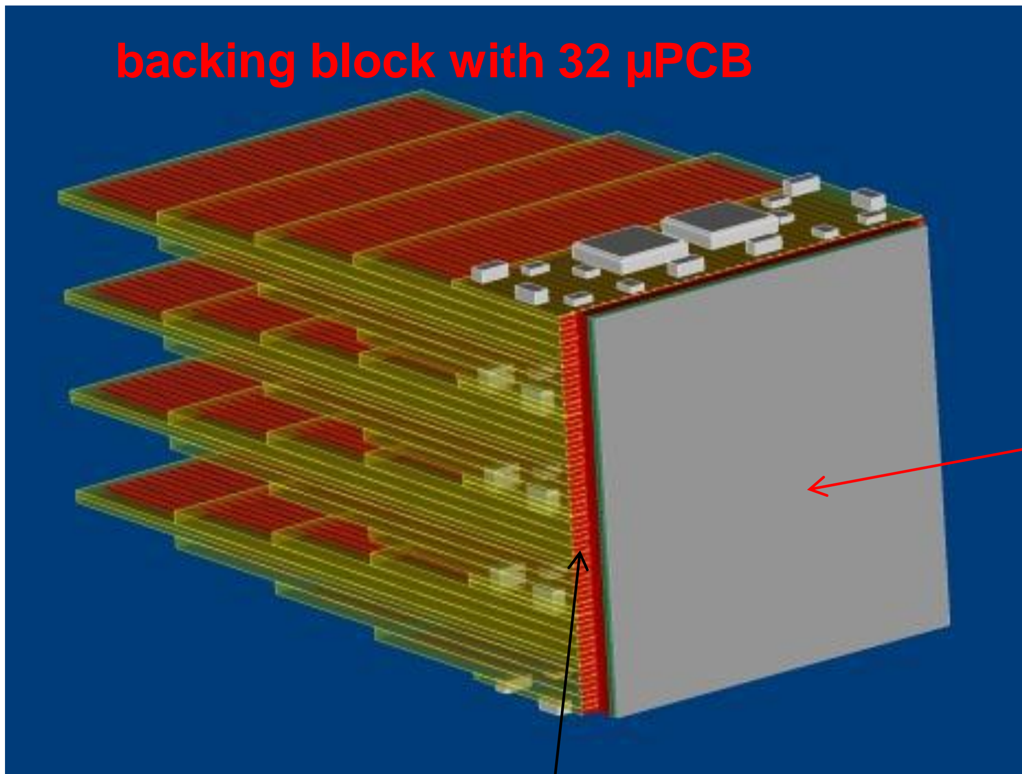
Medical Applications (6)

- **Dimensions : 2.3 x 5.2 x 7.3 mm**





Medical Applications (7)

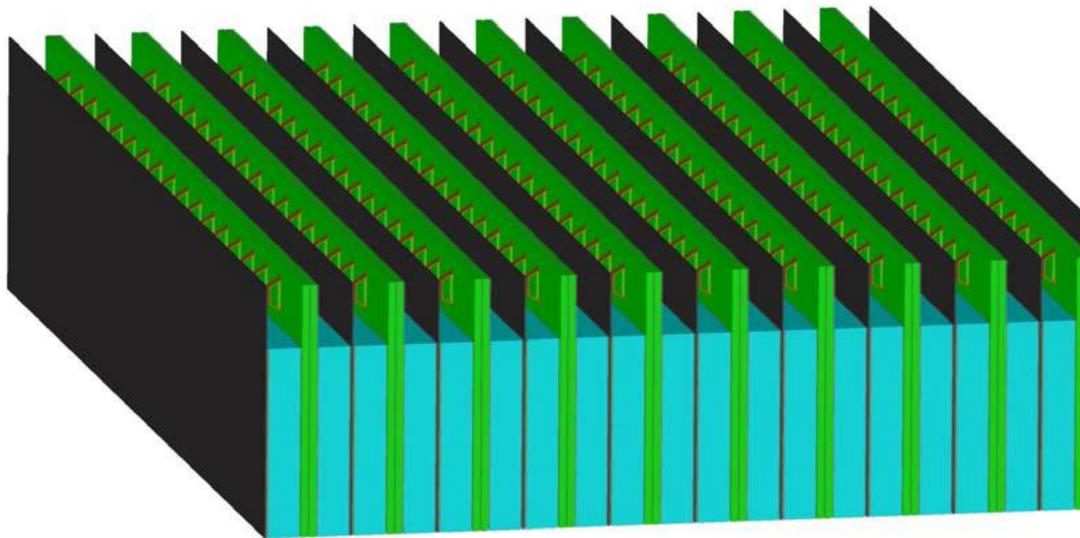


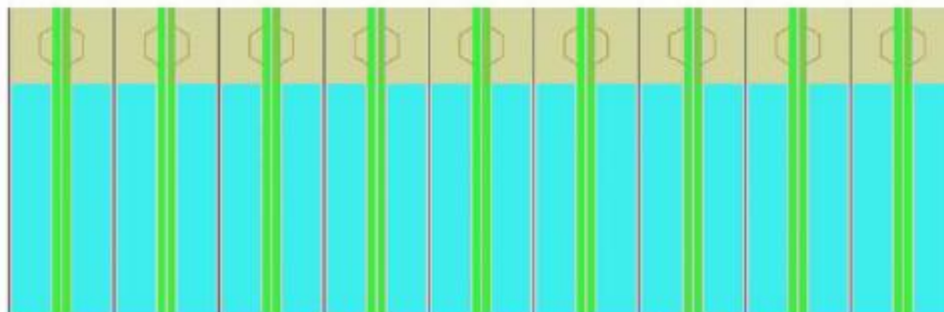
Ultrasonic probes
Applications
- Real time 3D ultrasonic imaging

Transducer array
- 64x64 elements
- **Array size : ≈28x28mm**

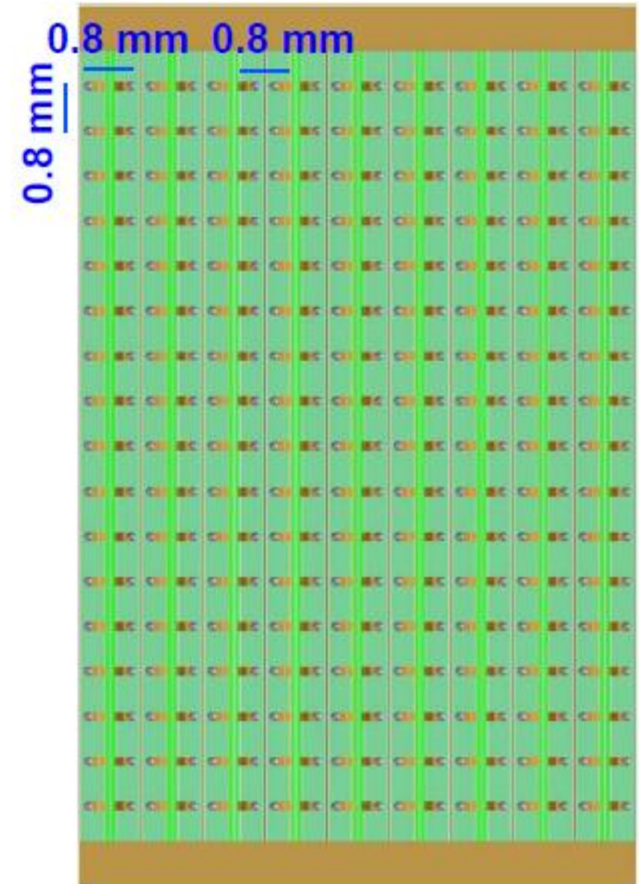
Interposer between transducer array and backing block

XRAY CdTe SENSOR FOR MEDICAL IMAGERY





side view



top view

plus 3D
a HEICO company

Outline

- Introduction
- Technology of the Stacking of Rebuilt Wafers
- Medical Applications
- Conclusions

Conclusions and perspectives

- Proof of Concept – completed (2002-2005)
  - European funding (25 M$) with CEA/LETI, AXALTO, ST Microelectronics, 3D PLUS, …
- Process Development & Optimization of WDoD (from 2006 up to Feb 2009) with NXP/Philips semiconductor
- From Feb 2009 Prototyping with the RCP Process from Freescale/Phoenix
- From Feb 2011 Prototyping with the e-WLB Process from Nanium (ex Quimonda) /Porto
- Functional Prototypes with DR3/JEDEC Qualifications

  (first Semester of 2013)
- Manufacturing Line for Prototypes and Small Volume Qualification (first Semester of 2013)

Conclusions and perspectives

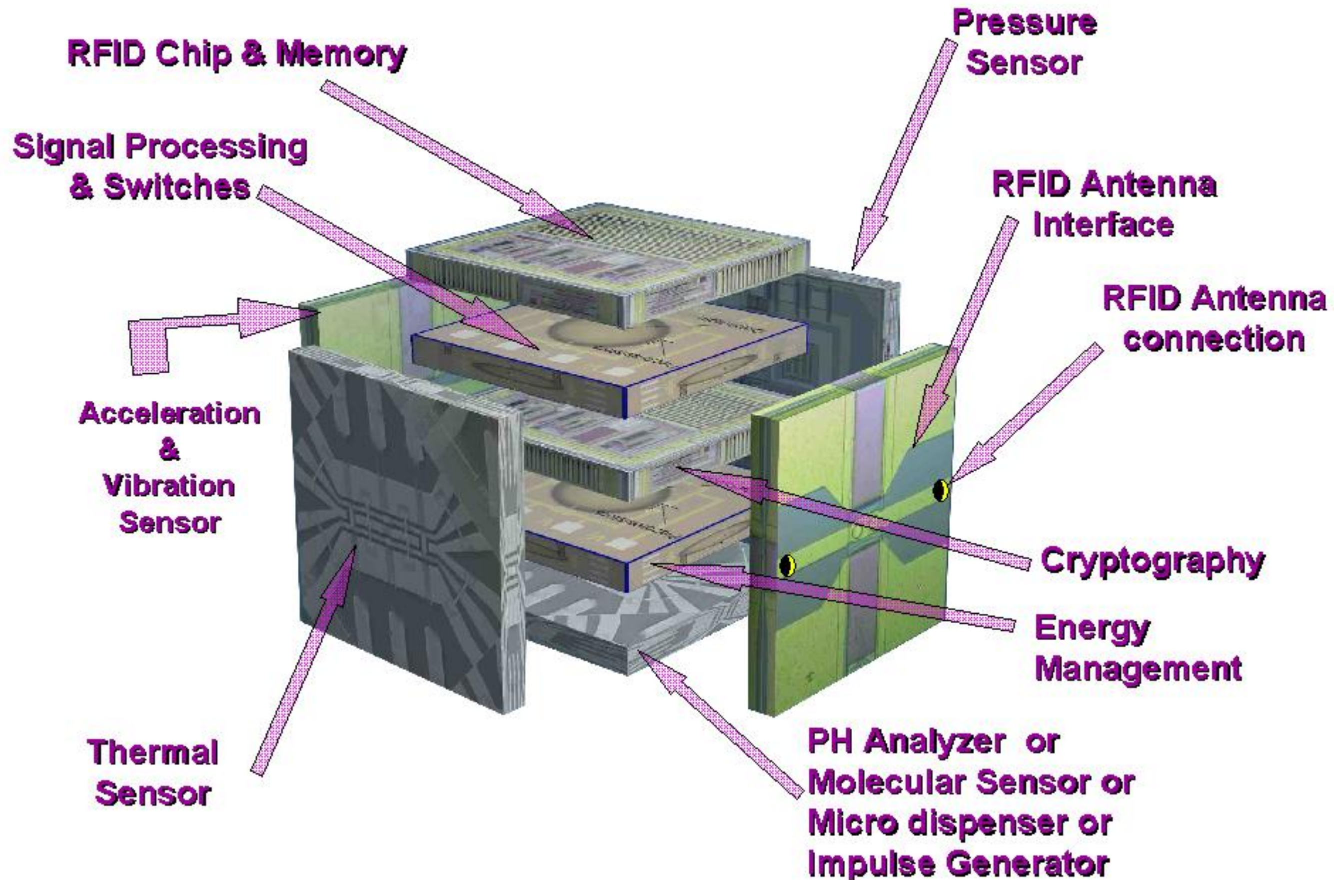
- **Miniaturization for Consumer, Medical and security domains demands very high interconnection densities and low costs . Reconsidering former experiences: Hybrids,Multichip Modules, Wafer Scale Integration (20 years ago), PoP instead of PiP; we learned that the yield constitued an important part of the production costs.**

- **The WDoD process only allows to stack Known Good Rebuilt Wafers .**

- **Several applications in the medical have been presented.**

- **This important densification of 10, soon 20 levels per mm, allows to launch extremely ambitious applications in the field of System in Package**

Conclusions and perspectives



Ultra Dense 3-D Micro system with WDoD

Thank you for your attention

www.3d-plus.com